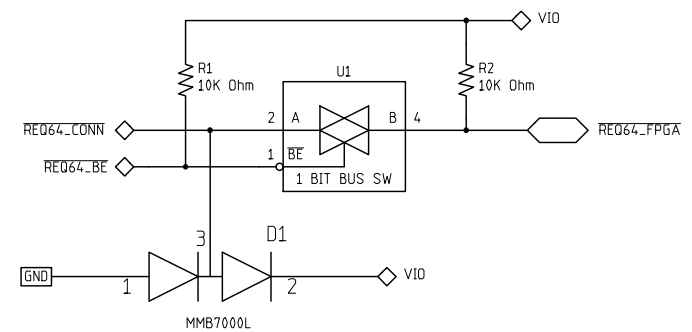
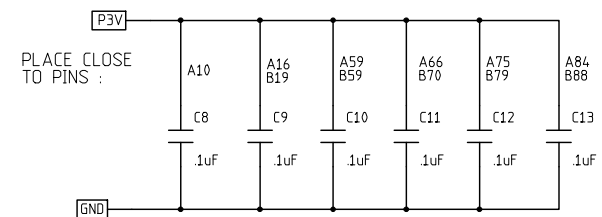
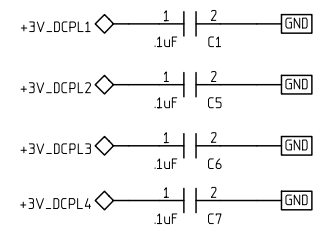
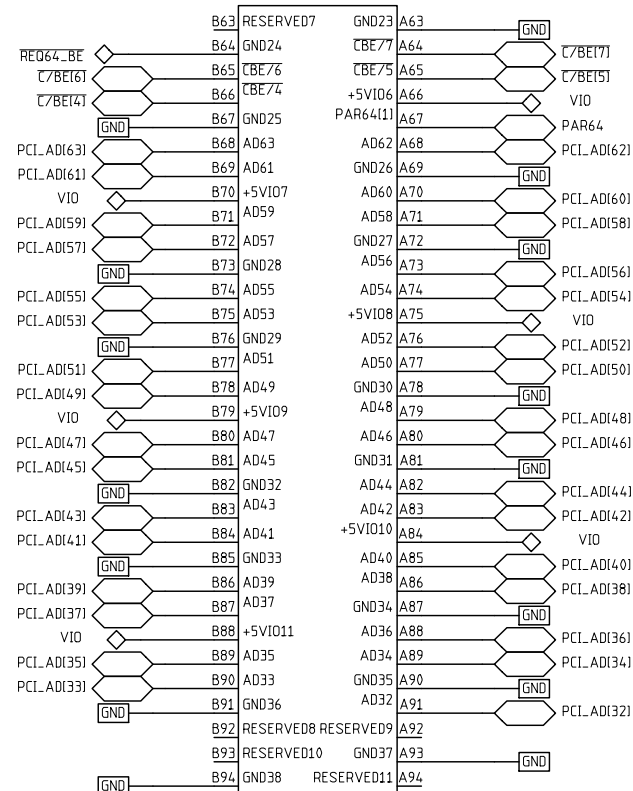
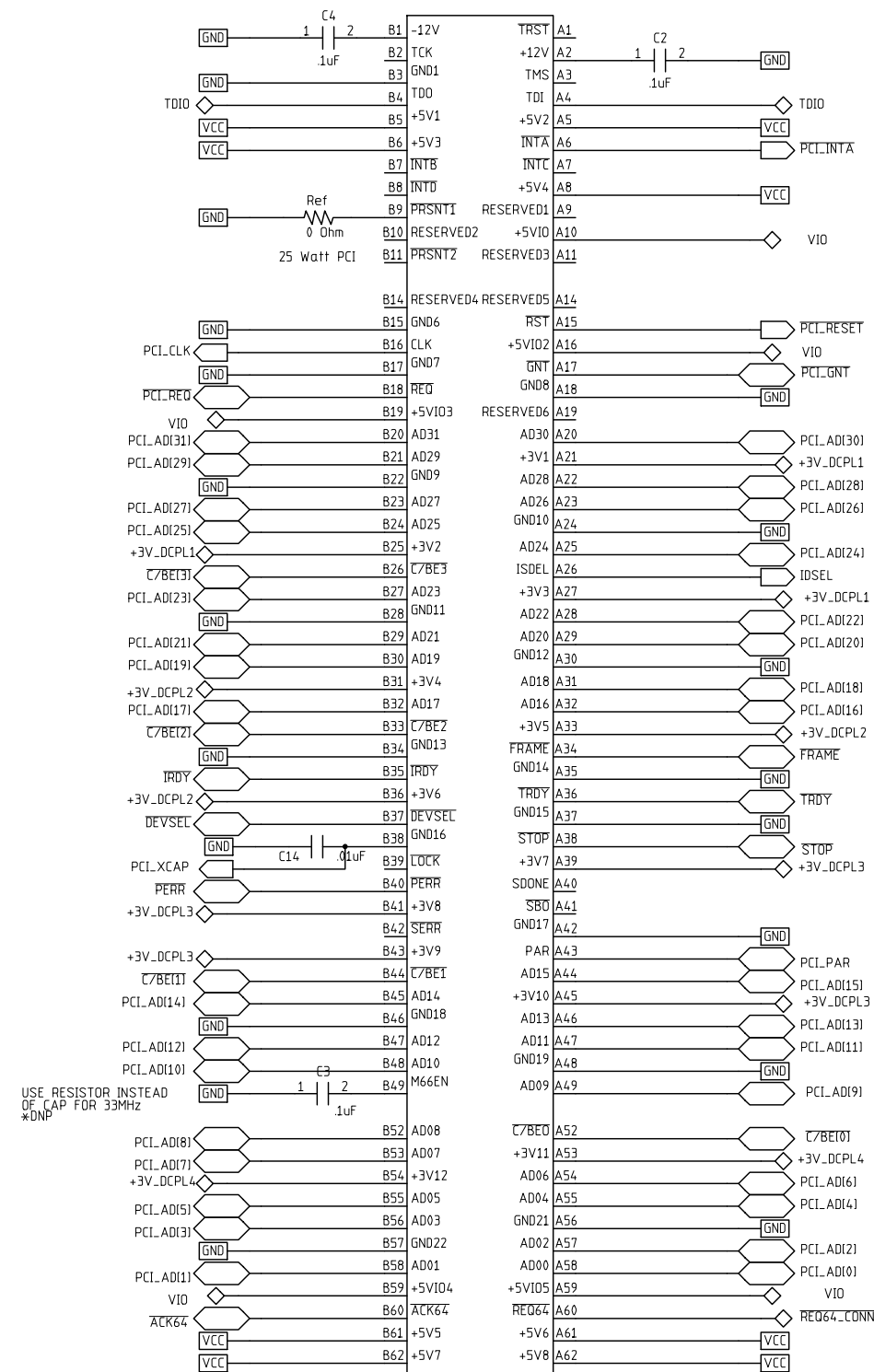
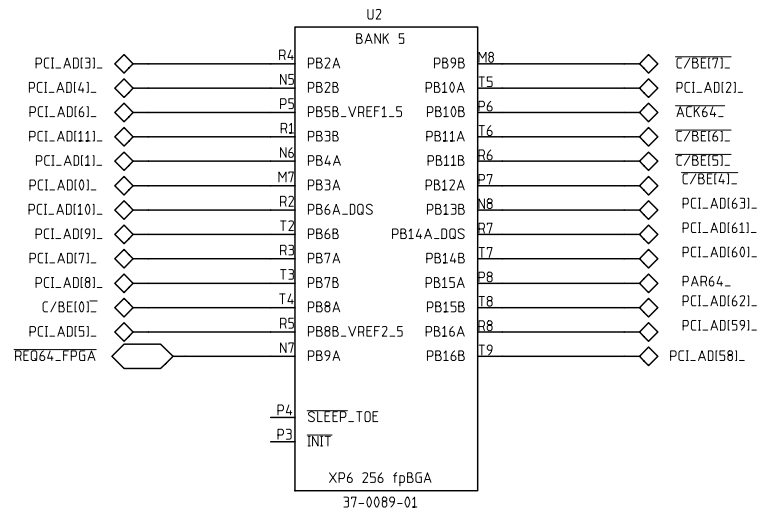
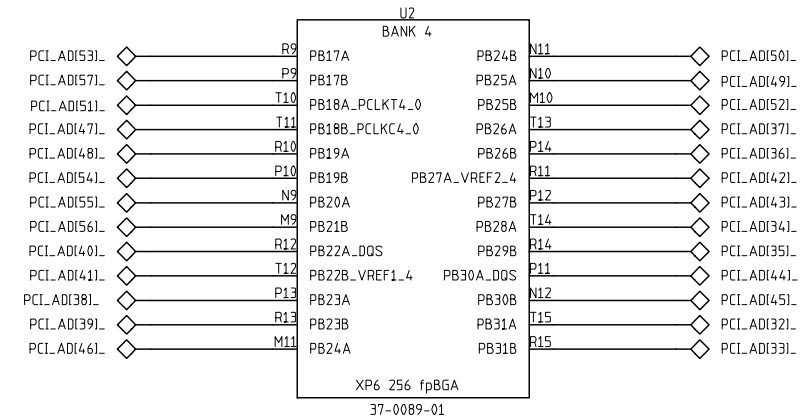
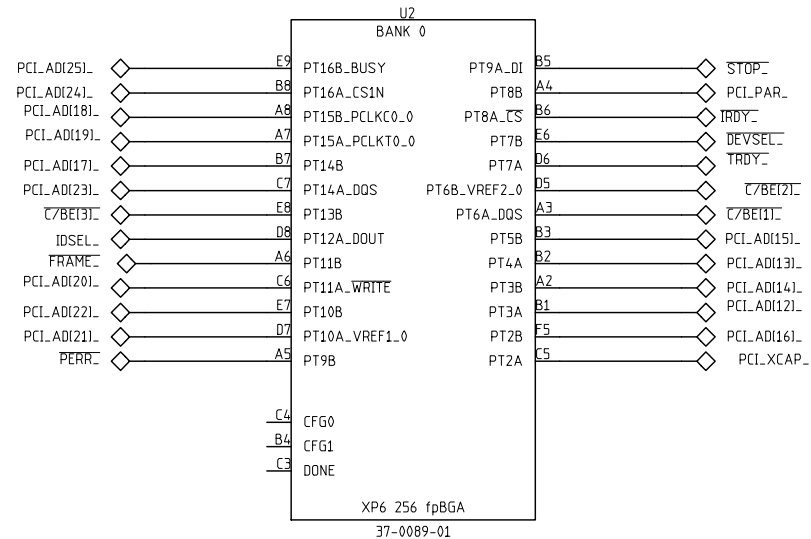
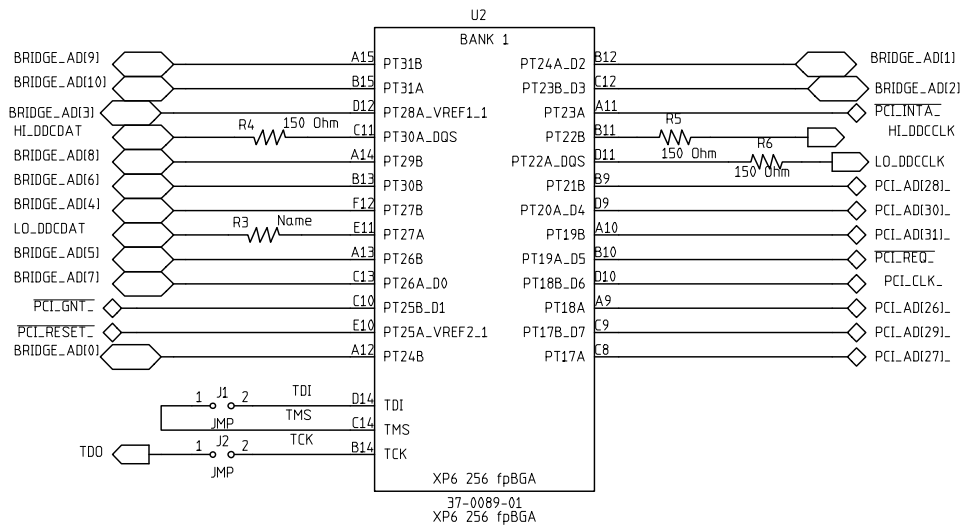
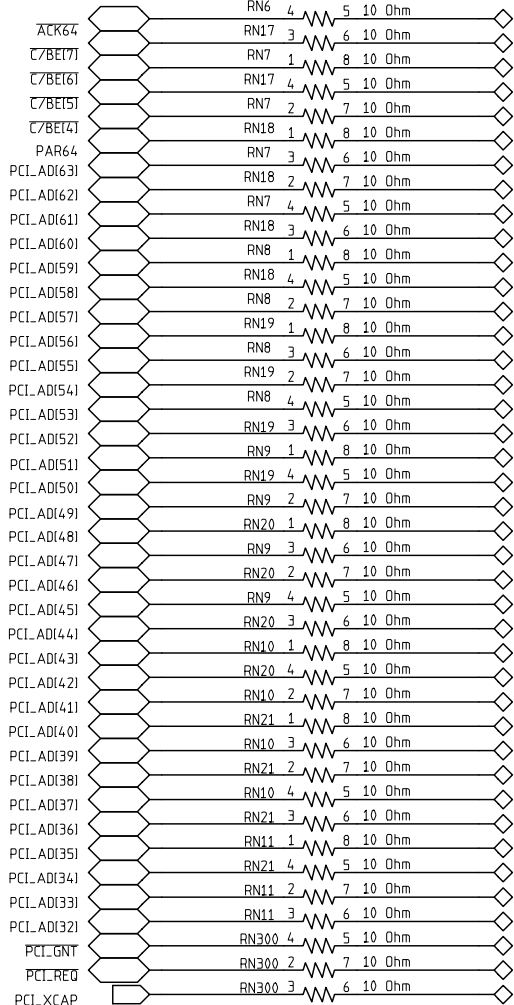
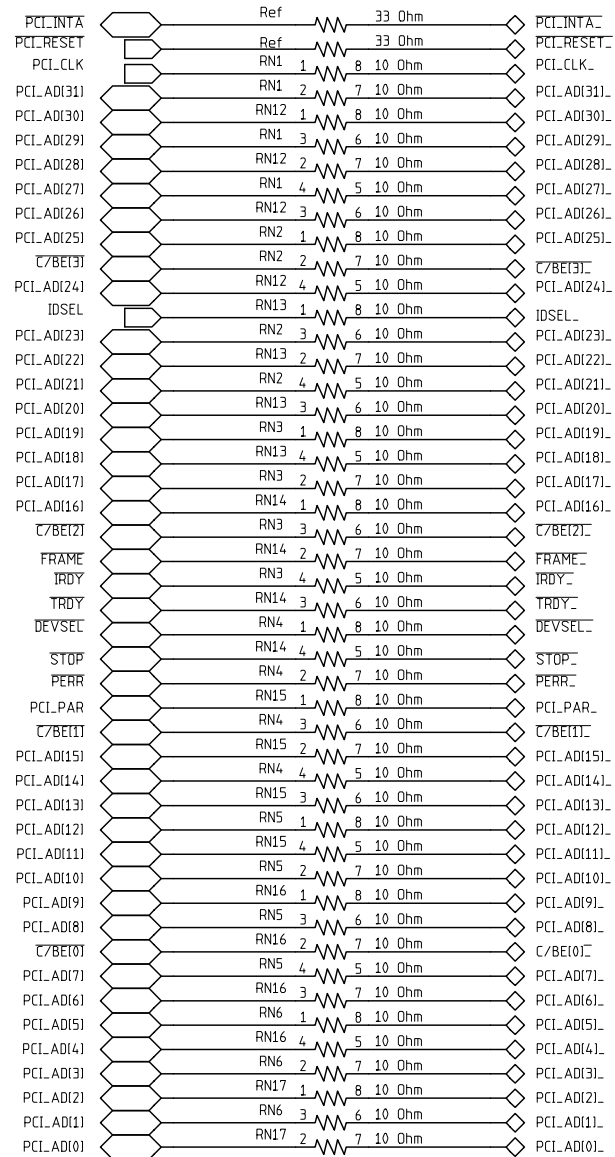


PCI CONNECTOR



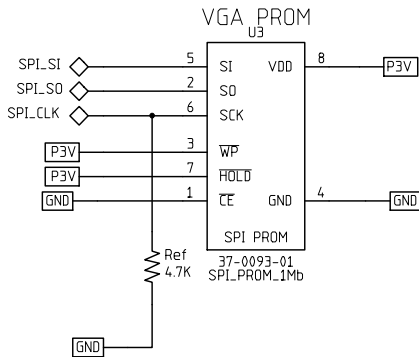
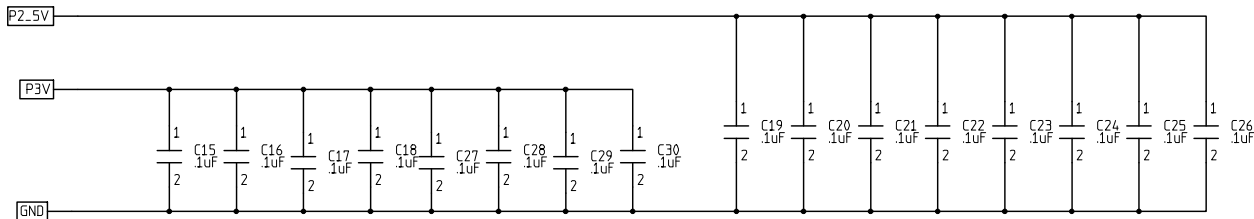
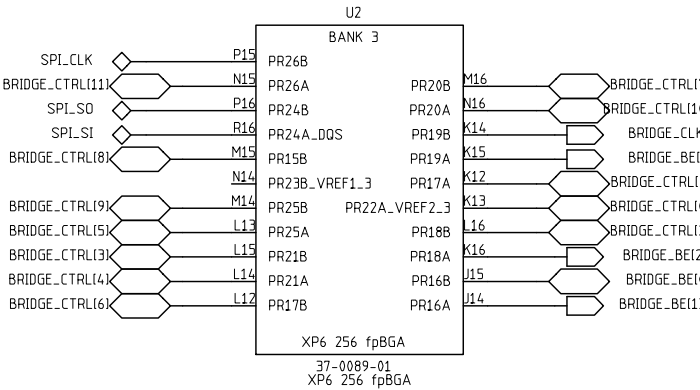
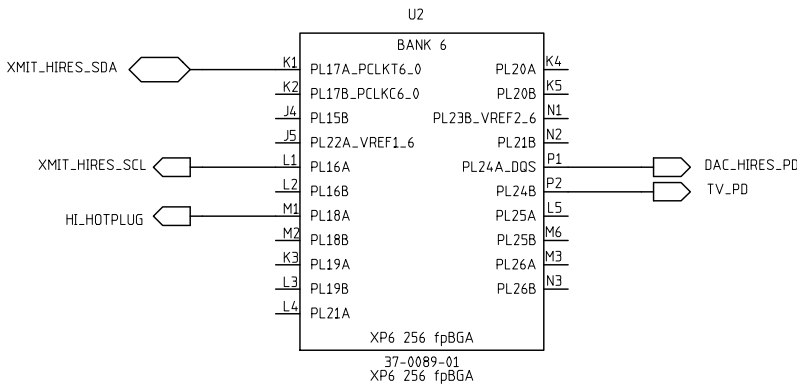
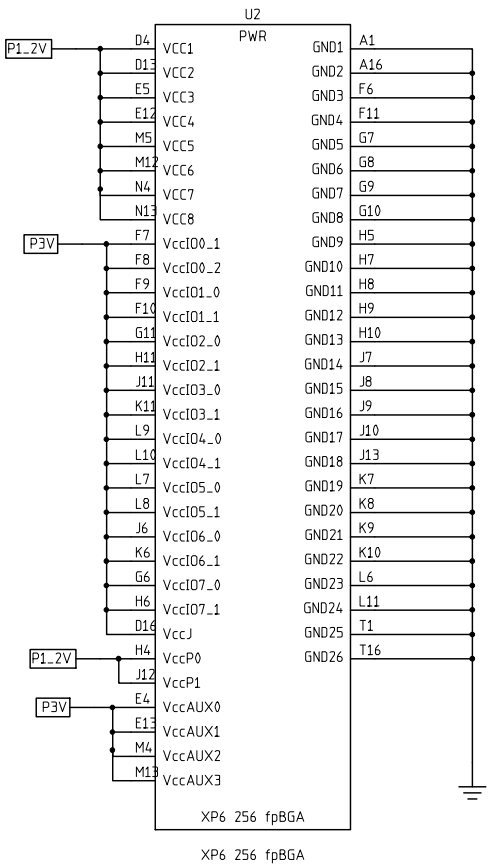
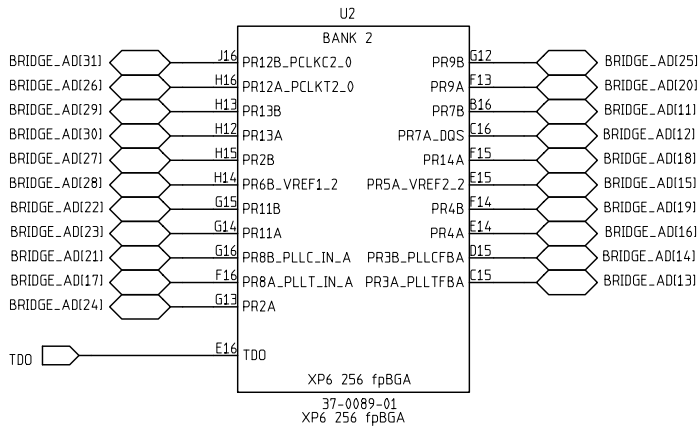
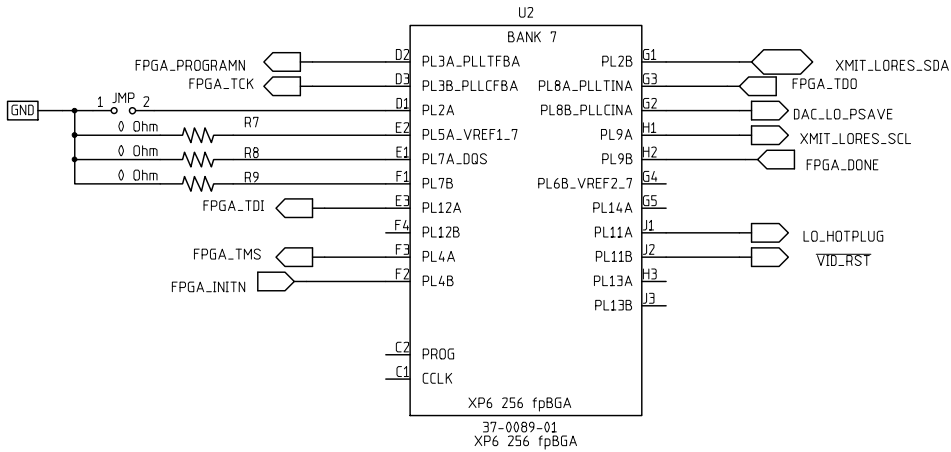
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ENG:					REV A
QA:			SCALE ~		SHEET 1 OF 18

XP6 PCI BRIDGE

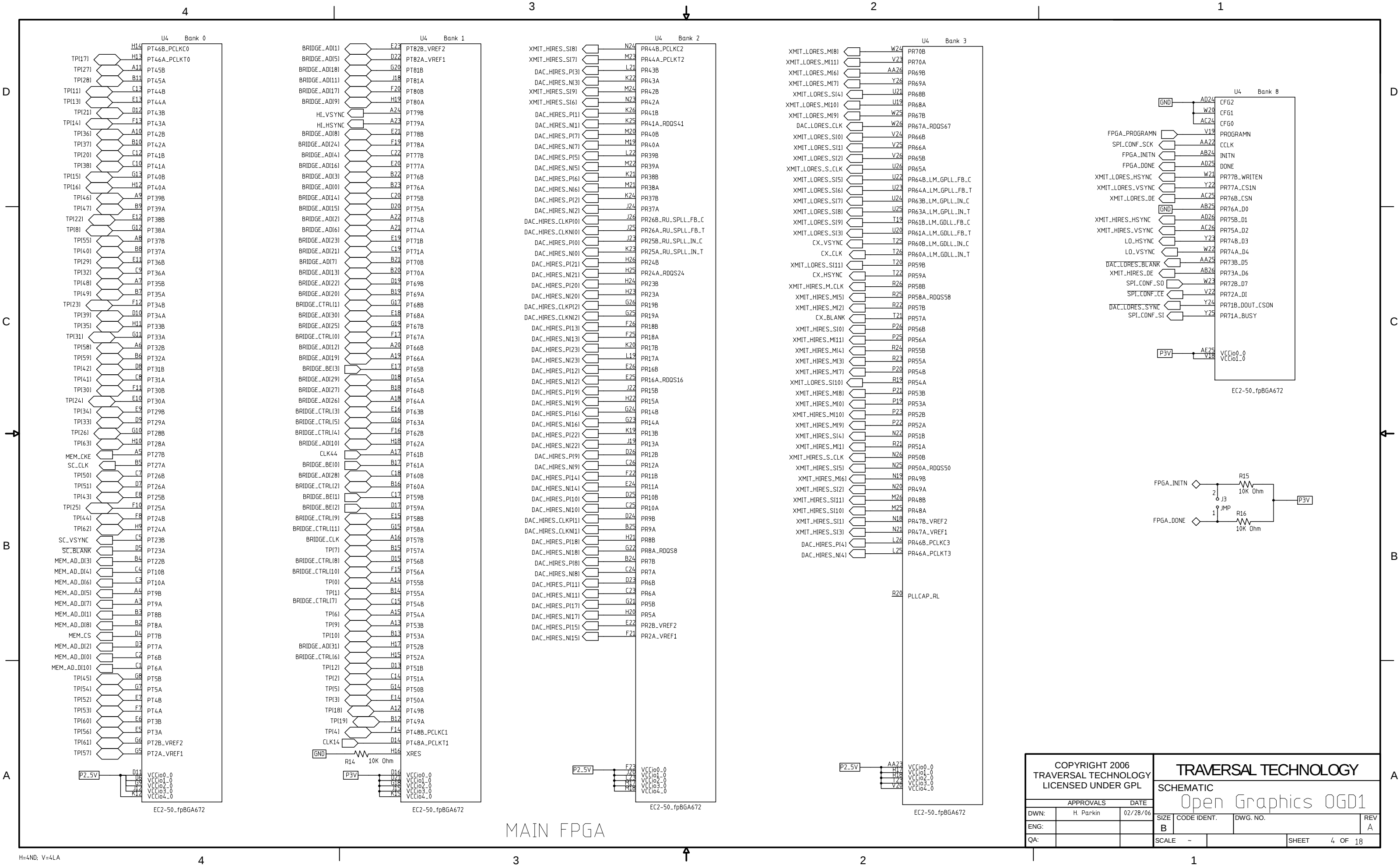


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QA:			SCALE	-	SHEET	2 OF 18

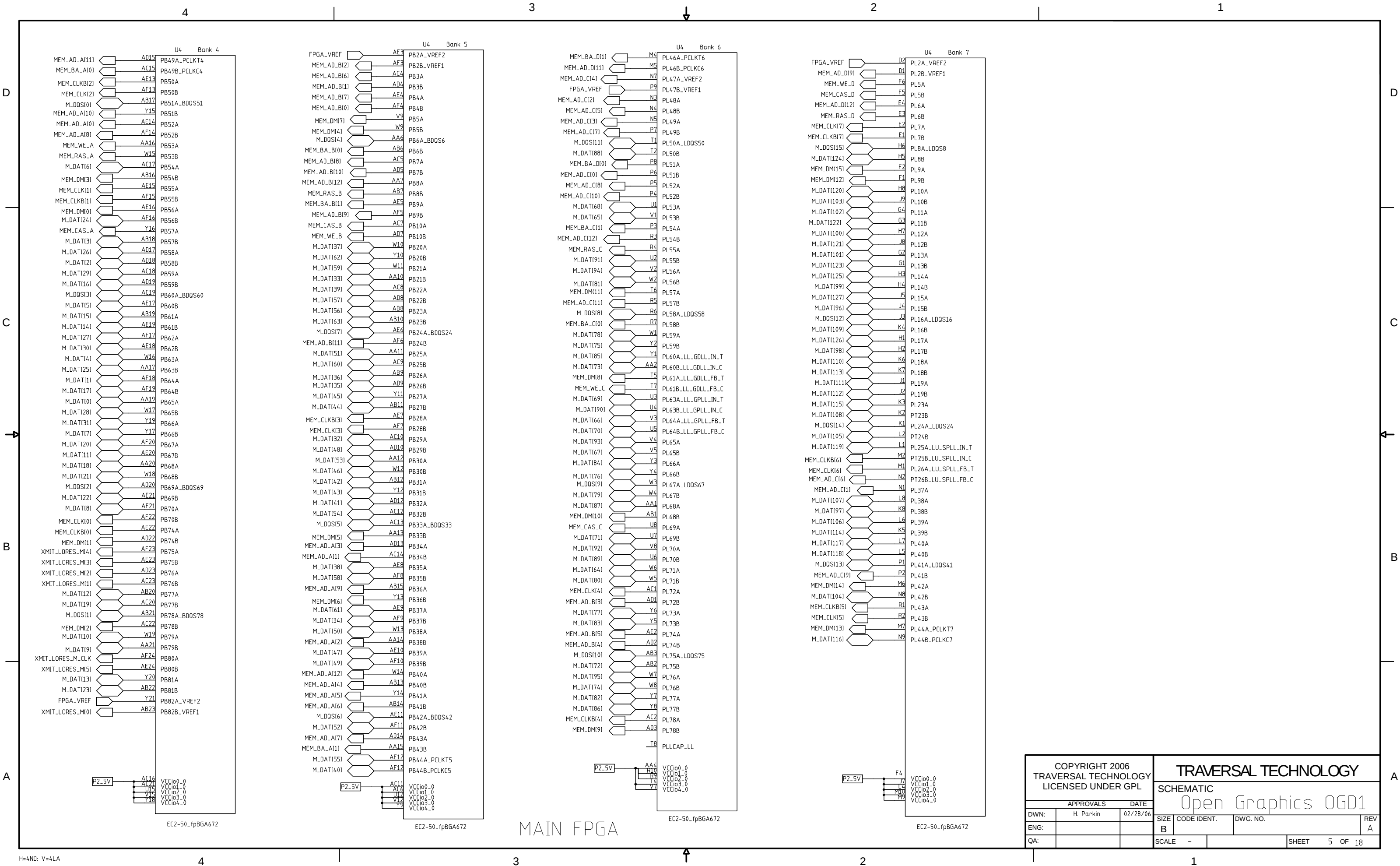
XP6 PCI BRIDGE



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QA:			SCALE	-	SHEET 3 OF 18

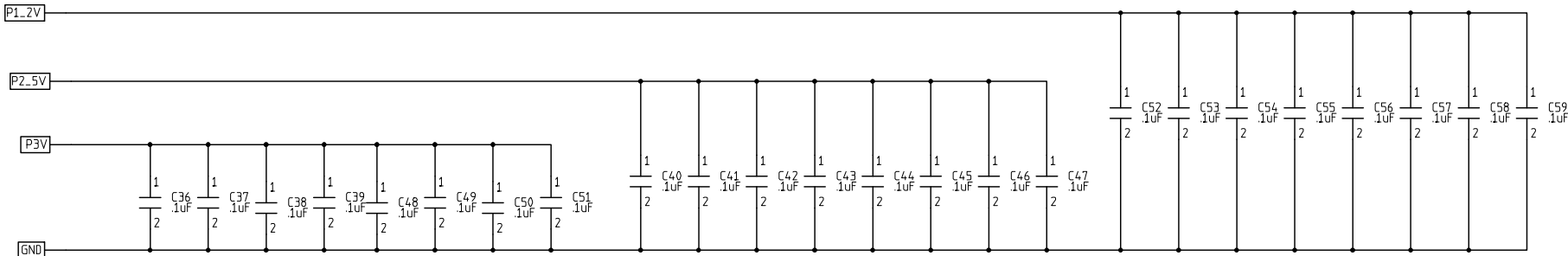
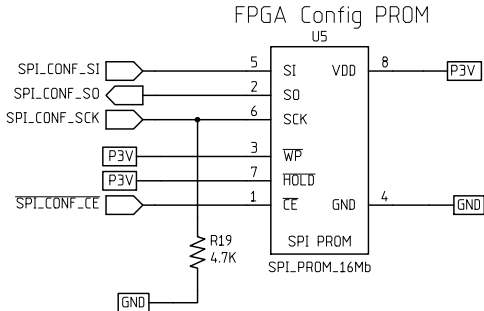
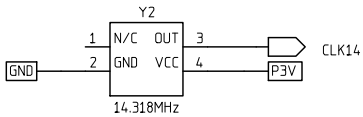
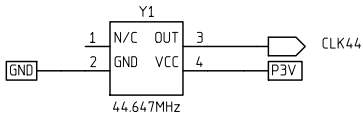
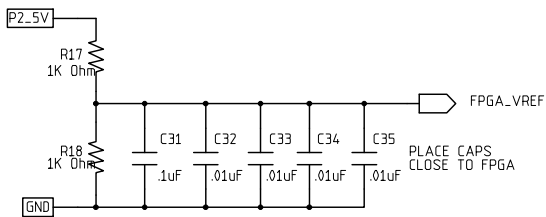
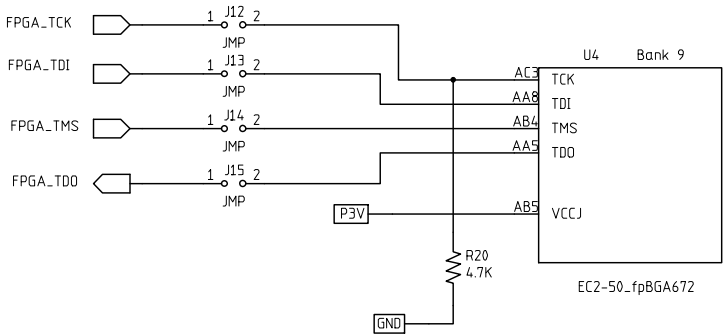
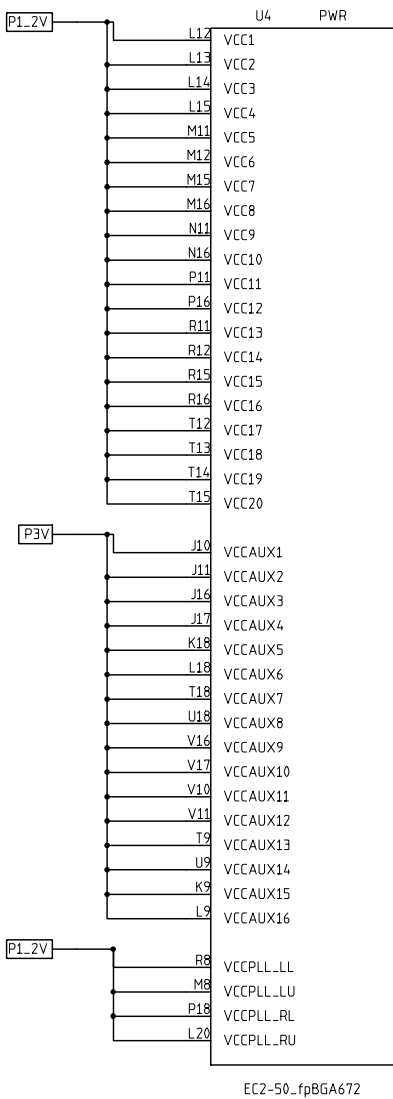


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QA:			SCALE	-	SHEET 4 OF 18

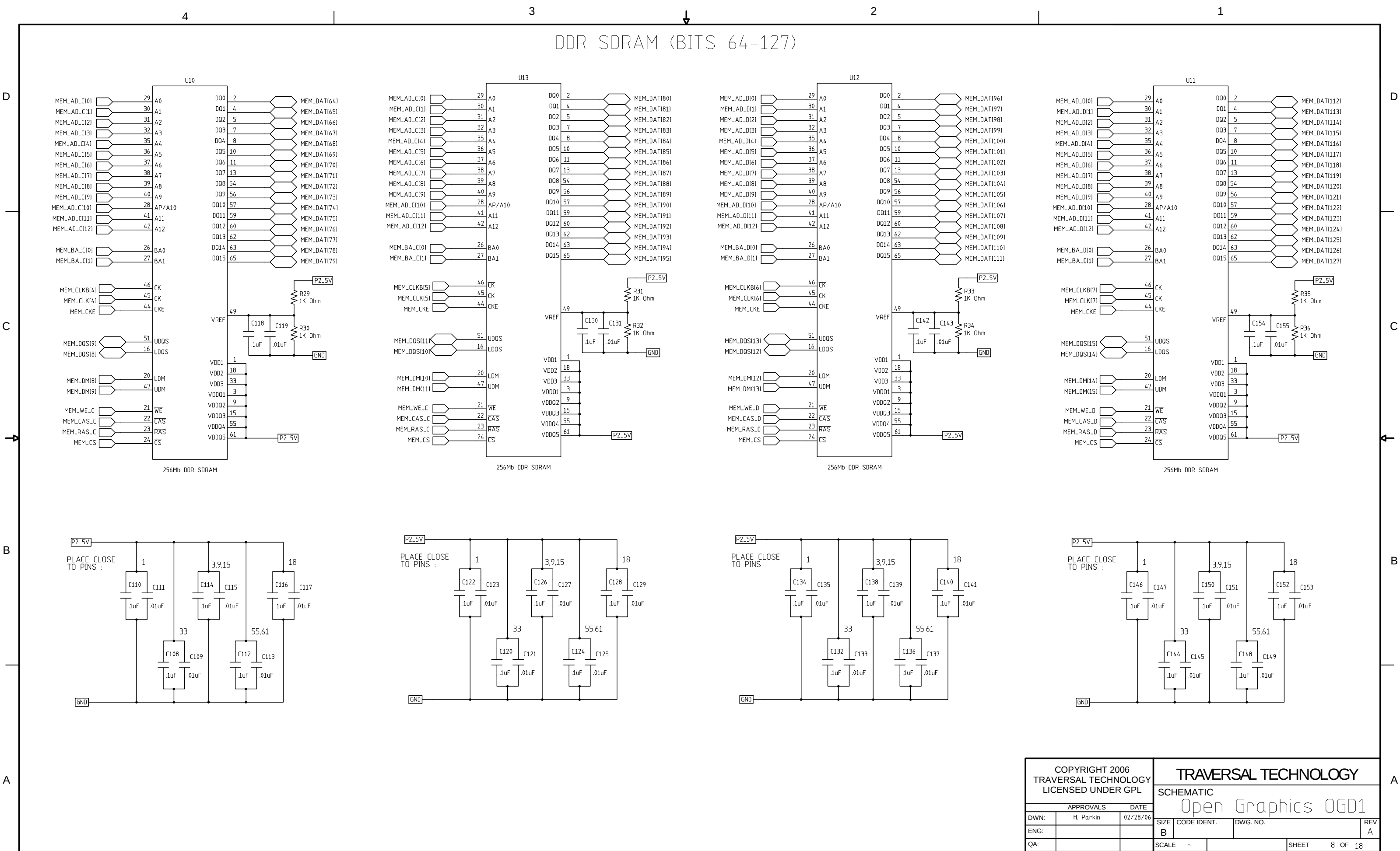


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			B		
SCALE			SHEET		
			5 OF 18		

MAIN FPGA POWER + SUPPORT DEVICES



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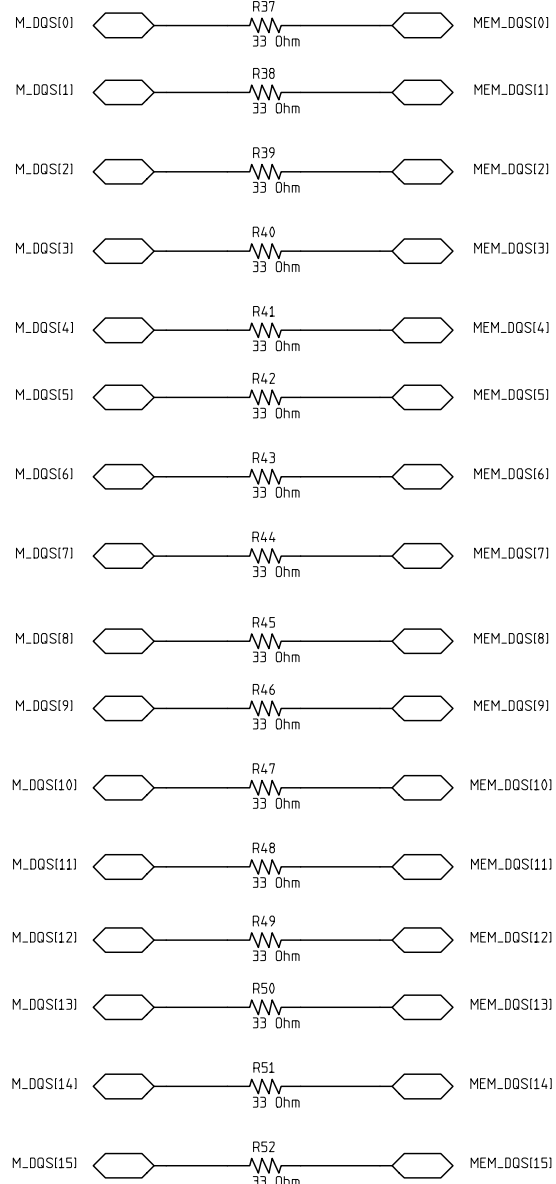
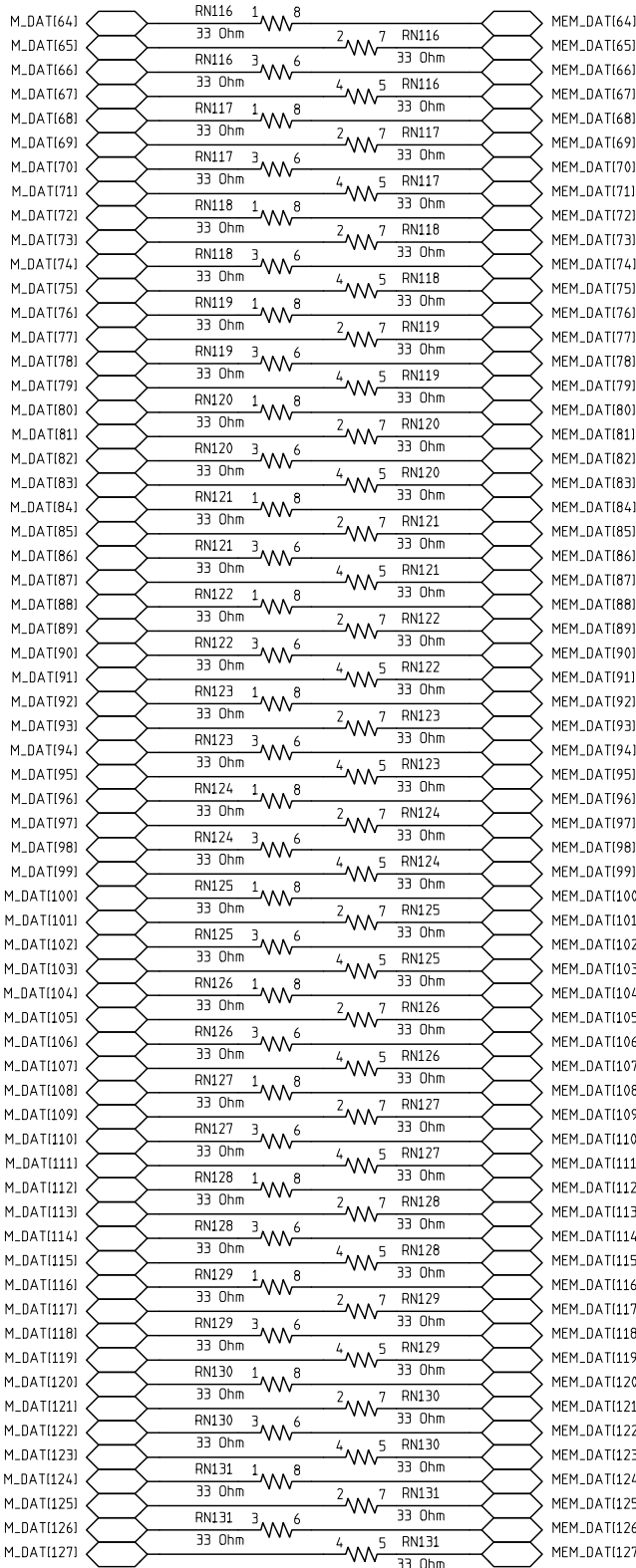
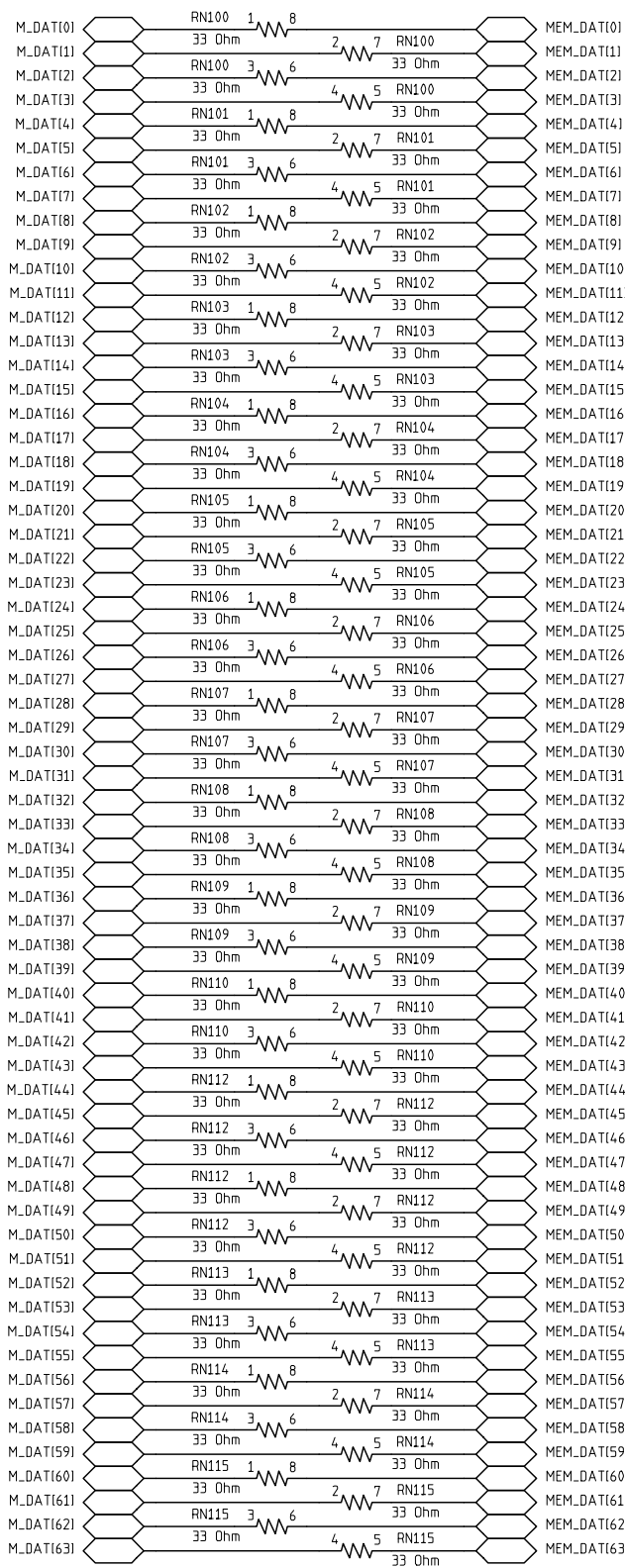
D

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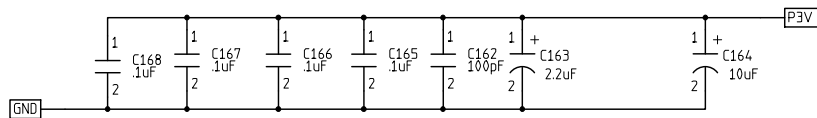
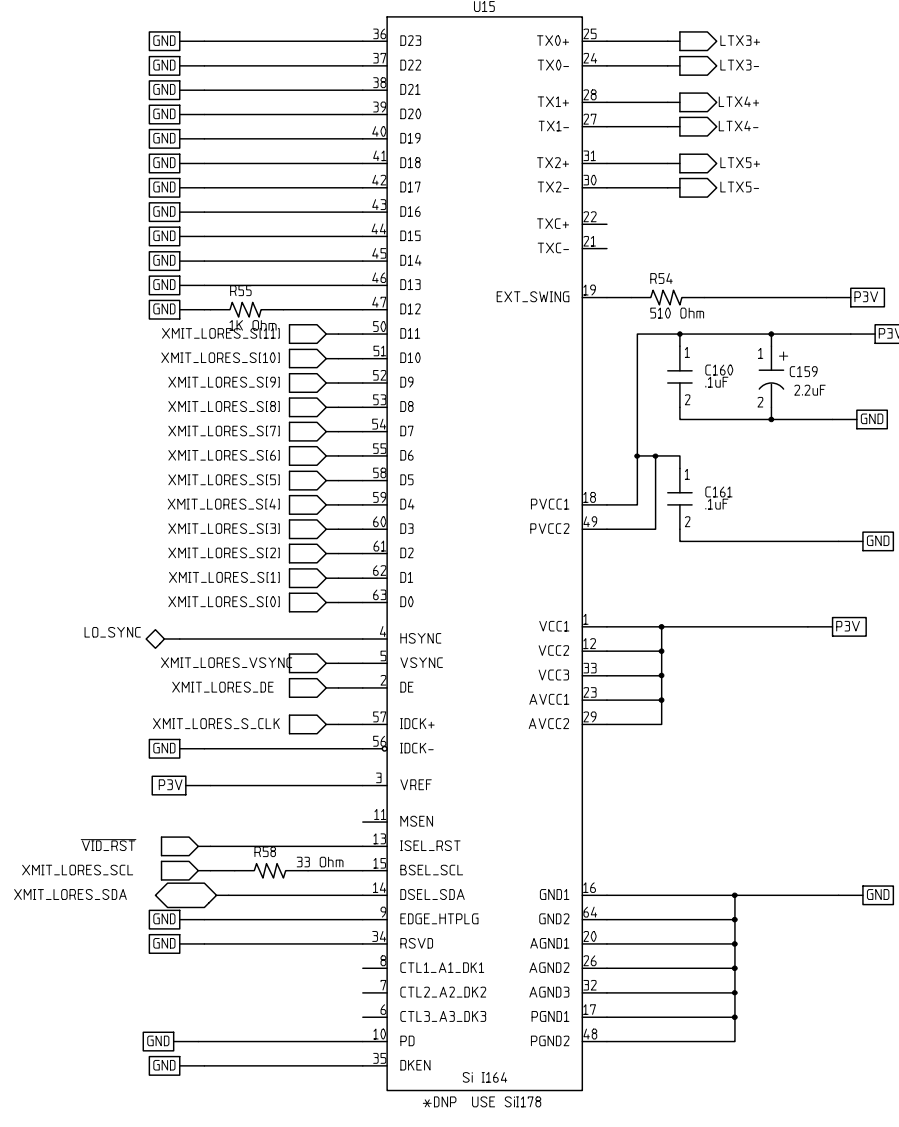
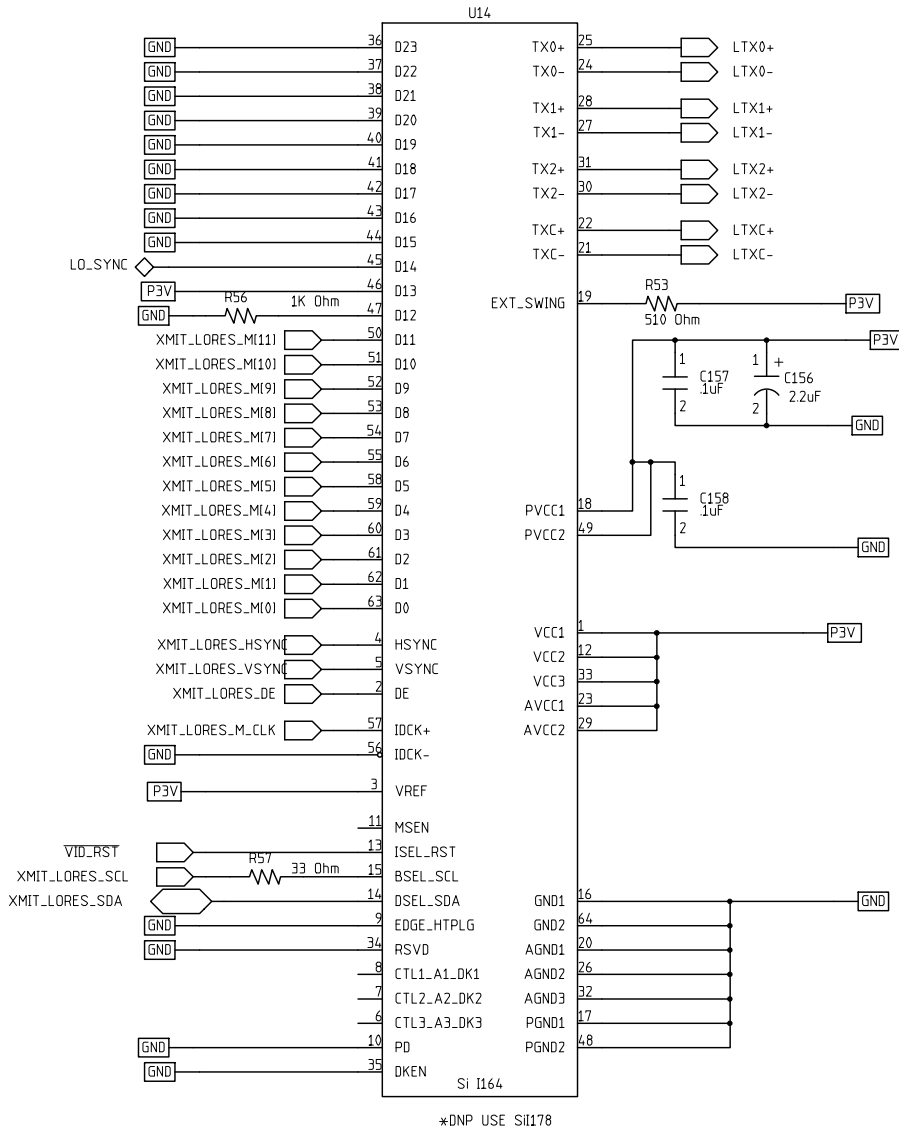
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DDR DATA/DQS TERMINATION



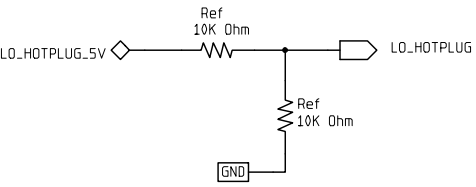
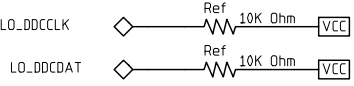
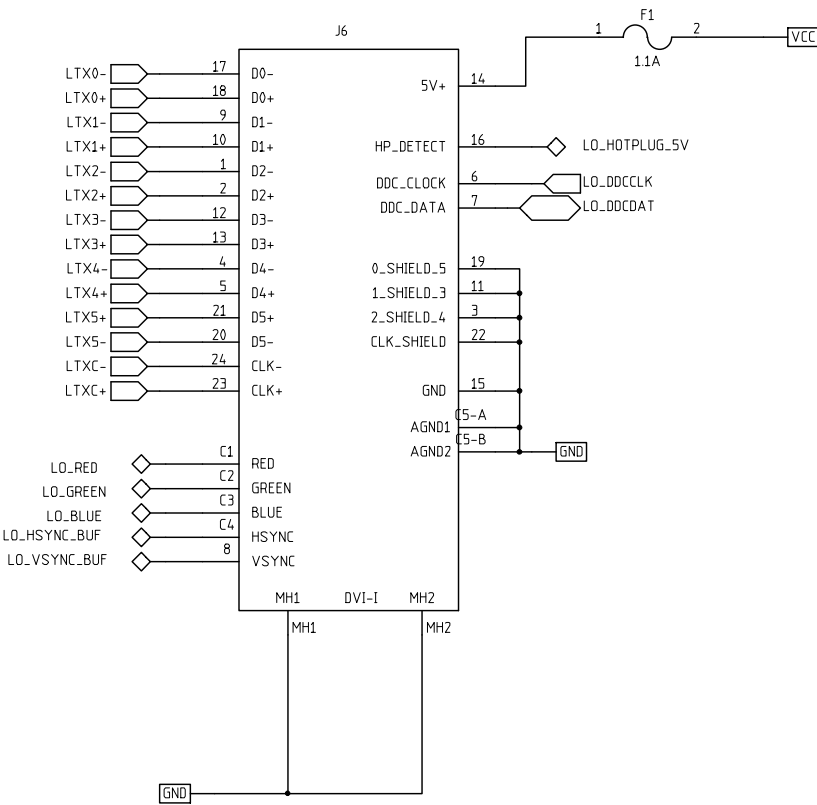
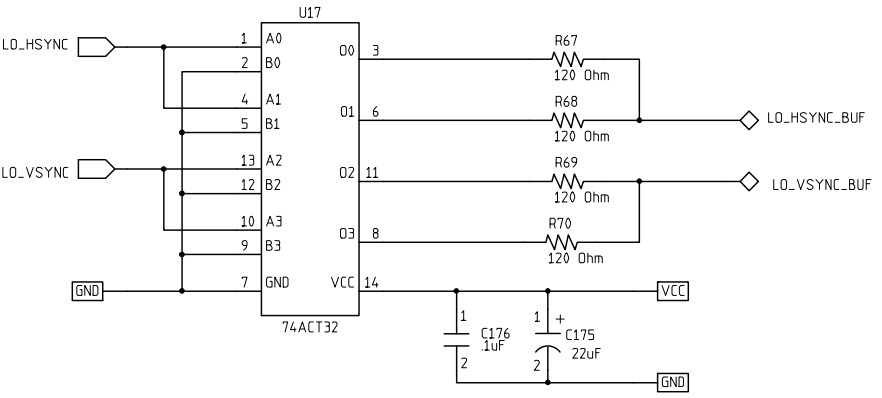
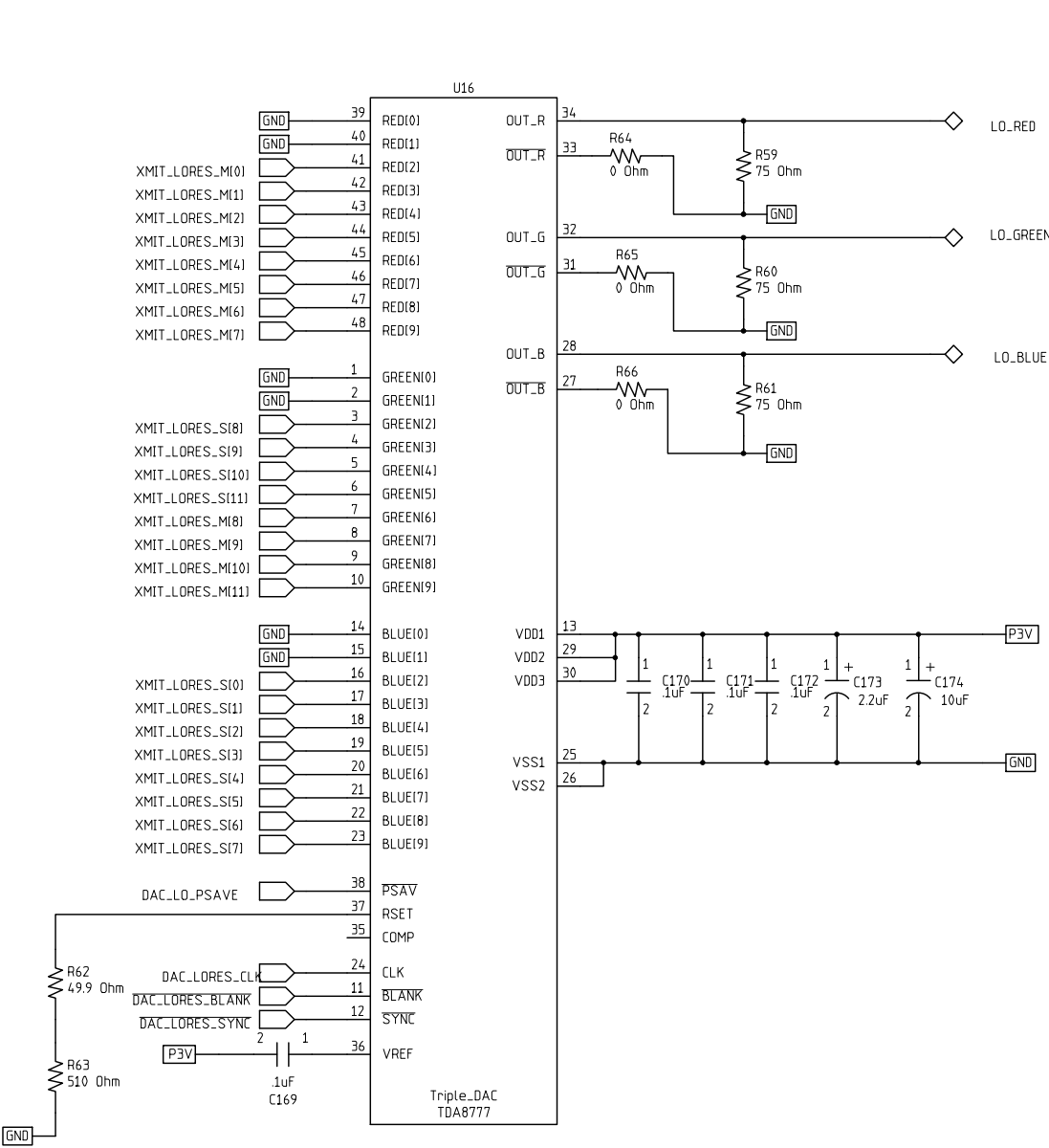
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QA:				B			A
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HEAD 1 DVI DUAL LINK



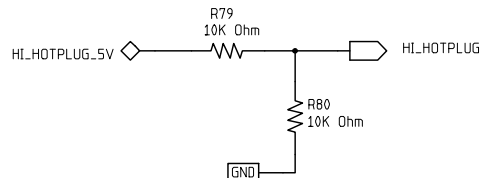
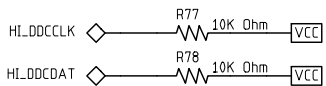
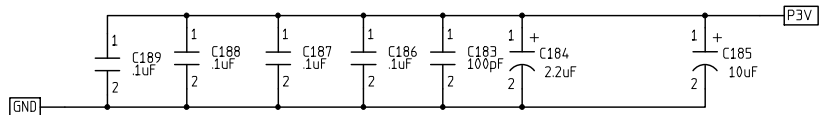
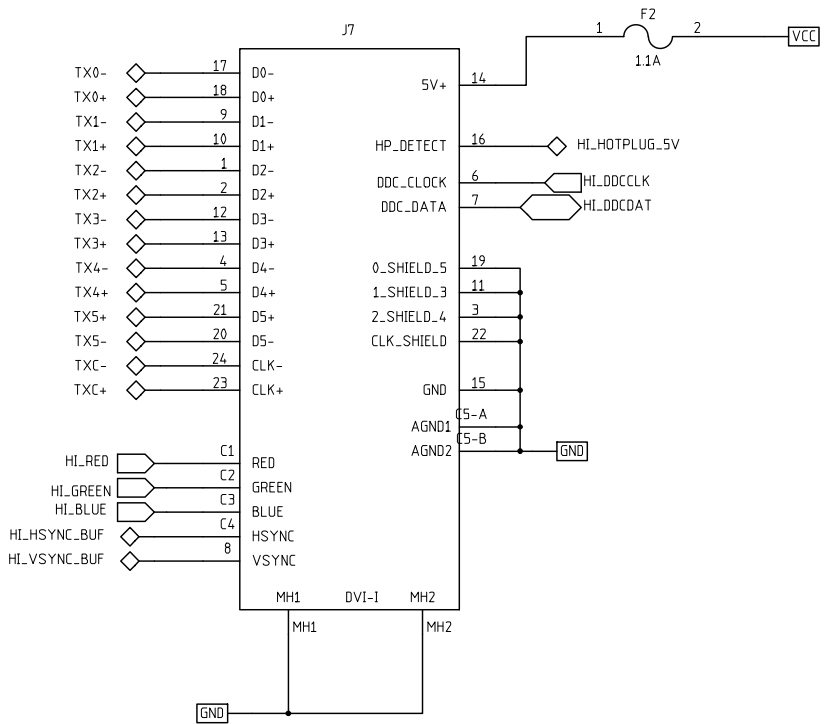
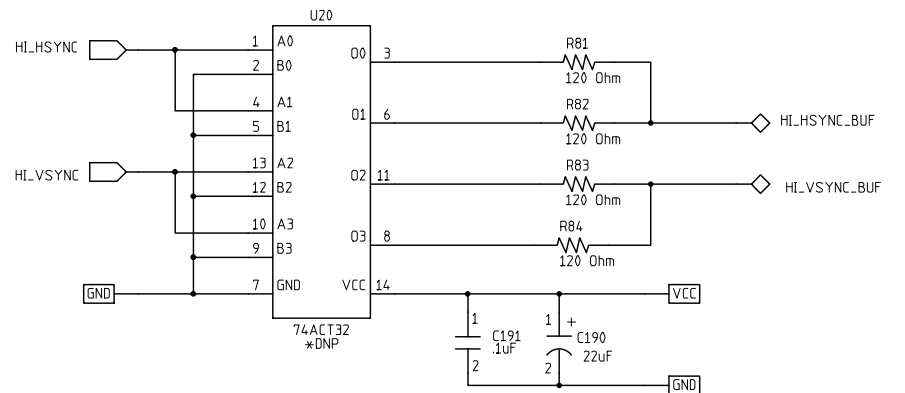
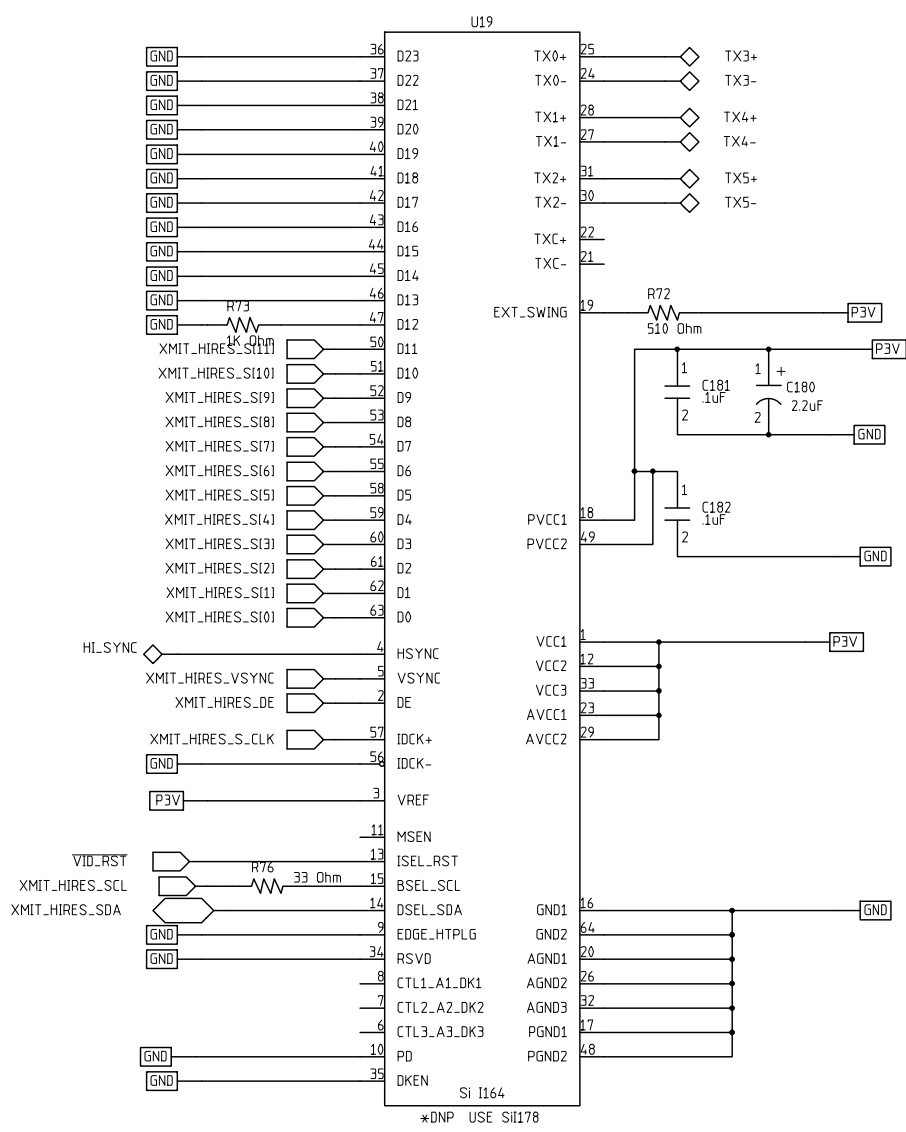
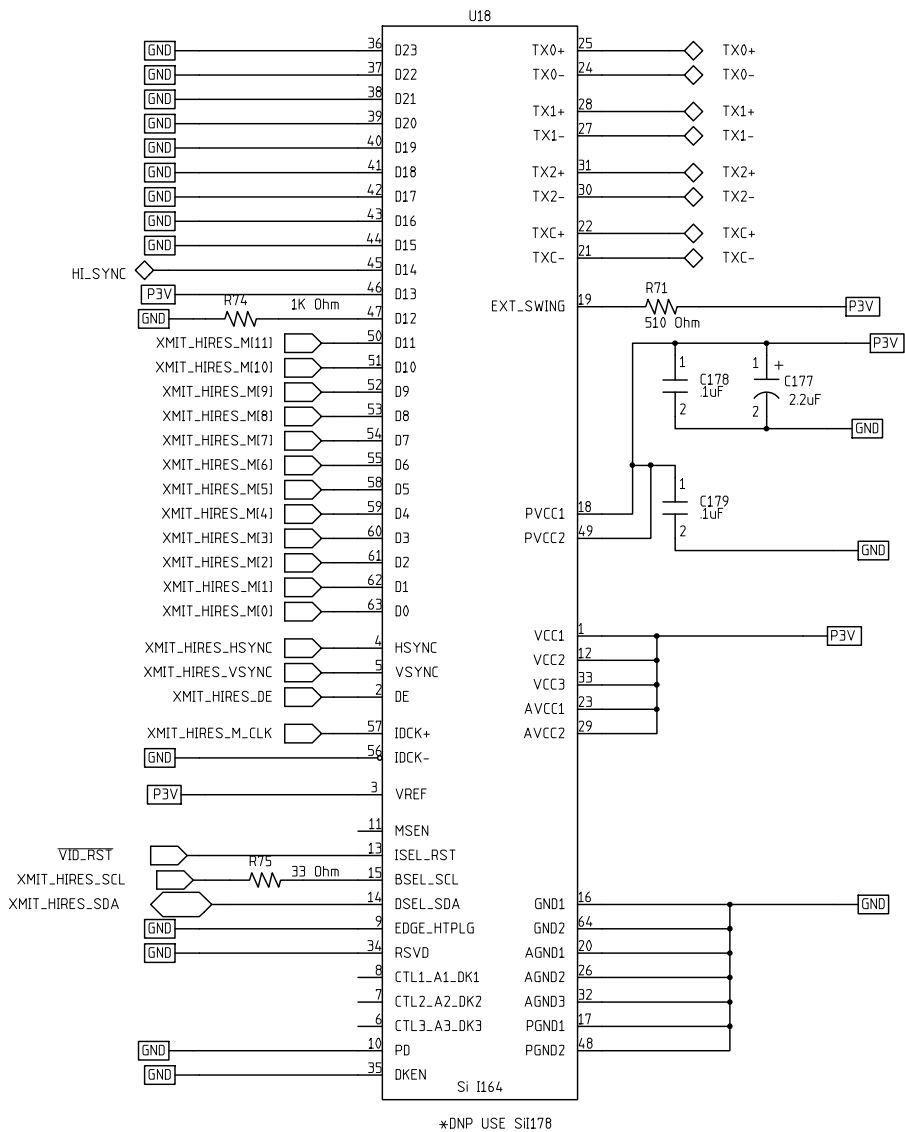
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			SCALE	-	SHEET 10 OF 18

HEAD 1 VGA OUTPUT



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HEAD 2 DVI DUAL LINK



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ENG:			B		
QA:			SCALE	-	SHEET 12 OF 18

Open Graphics OGD1

REV A

D

C

B

A

D

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J8

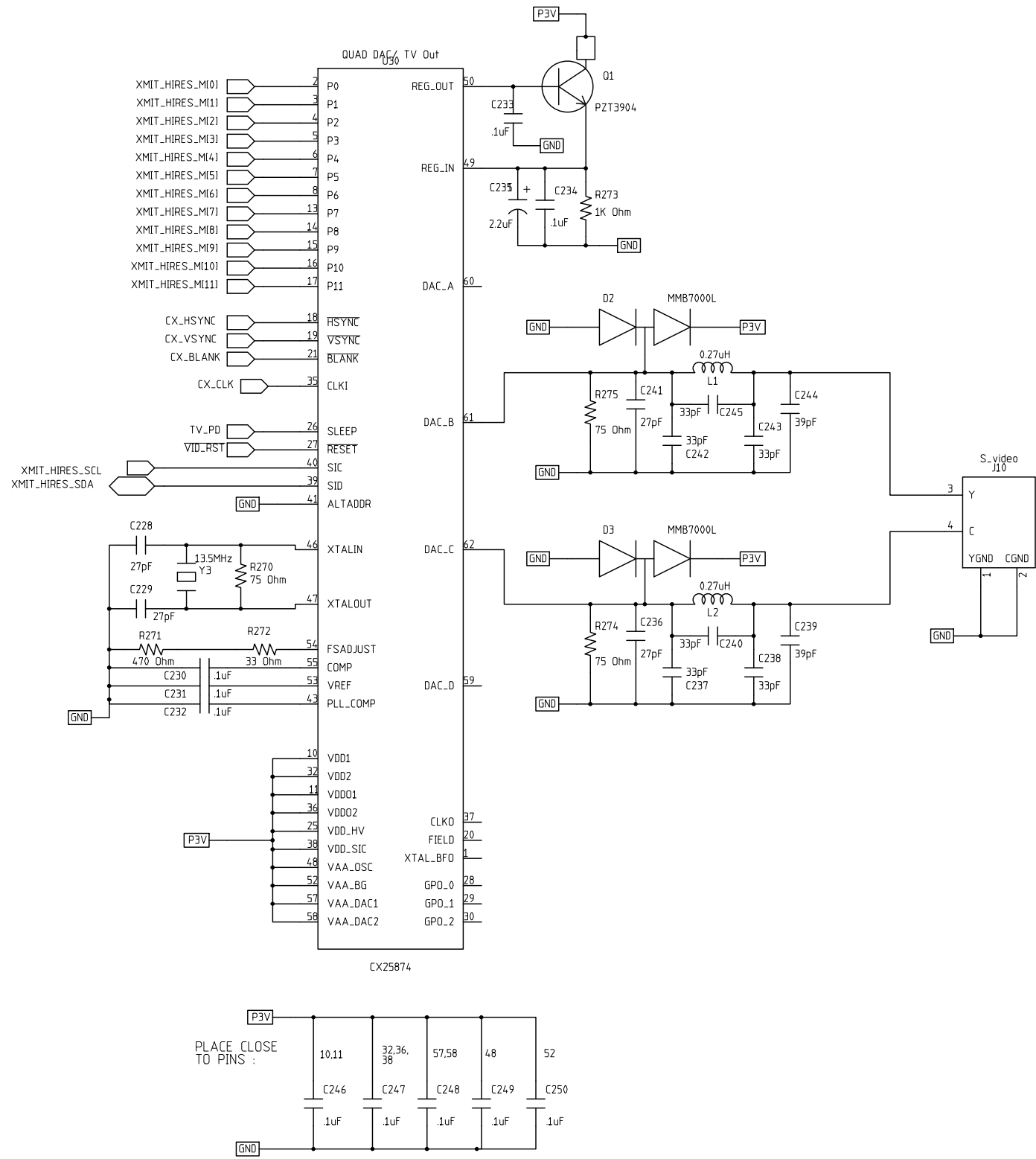
P50E

Place Resistors Close To FPGA

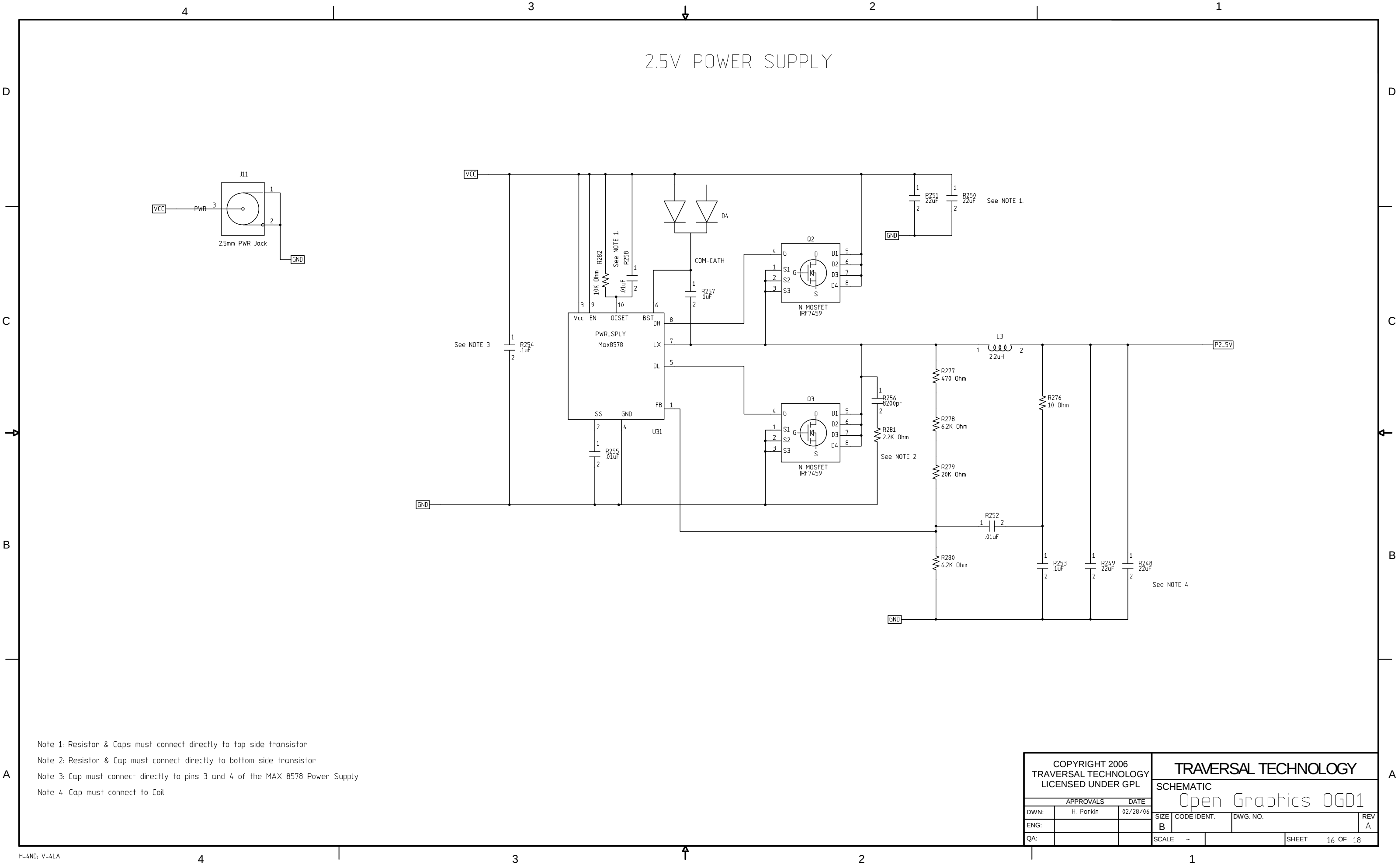
GENERAL PURPOSE I/O

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SCALE			-	SHEET 14 OF 18	

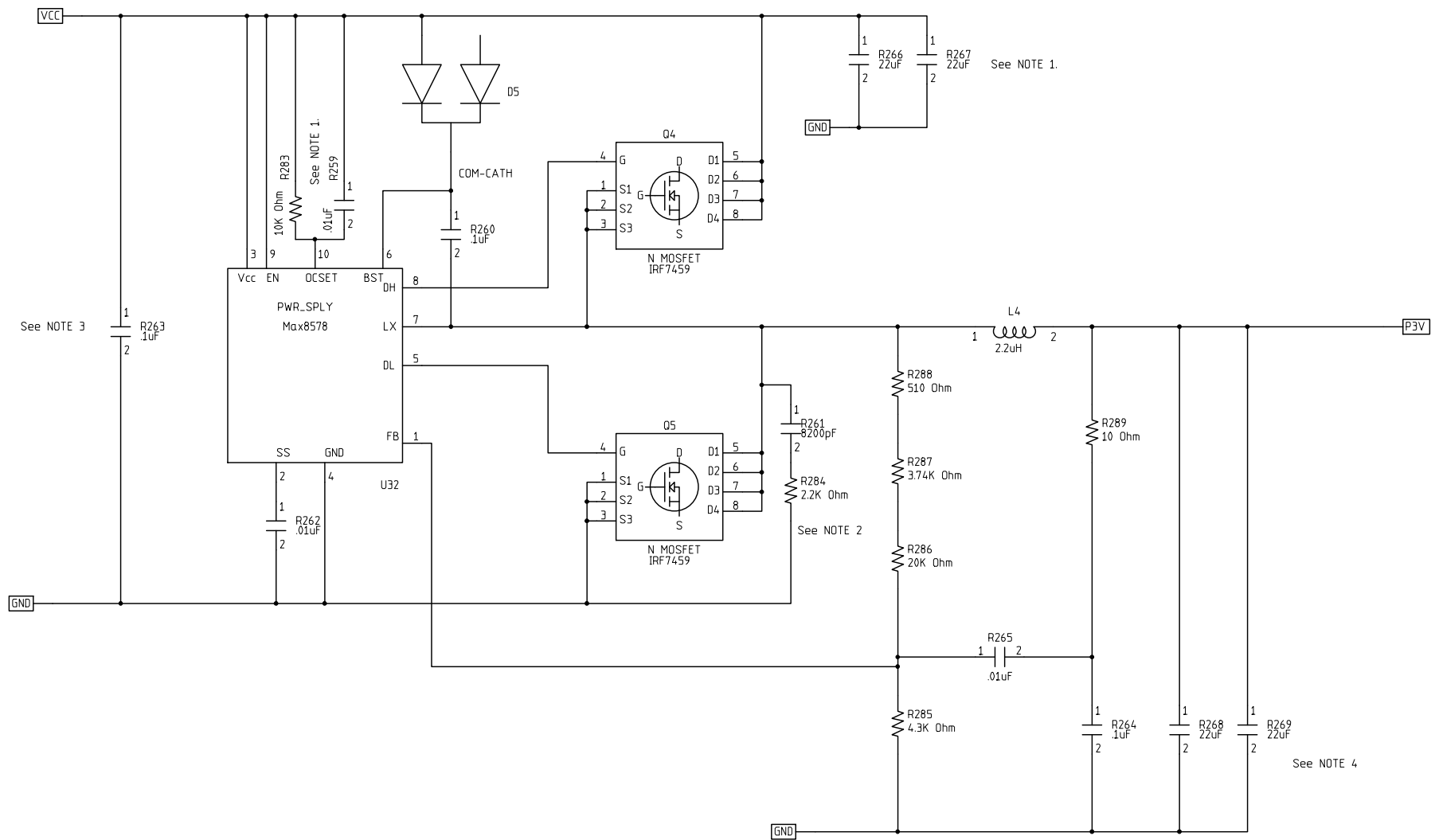
TV OUT



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ENG:			B			A
QA:			SCALE	-	SHEET	15 OF 18



3.3V POWER SUPPLY



Note 1: Resistor & Caps must connect directly to top side transistor
Note 2: Resistor & Cap must connect directly to bottom side transistor
Note 3: Cap must connect directly to pins 3 and 4 of the MAX 8578 Power Supply
Note 4: Cap must connect to Coil

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DATE			Open Graphics OGD1			
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ENG:			B			A
QA:			SCALE	-	SHEET	17 OF 18

D



A

A