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Flash Memory Testing

Model 4200-Flash

Introduction

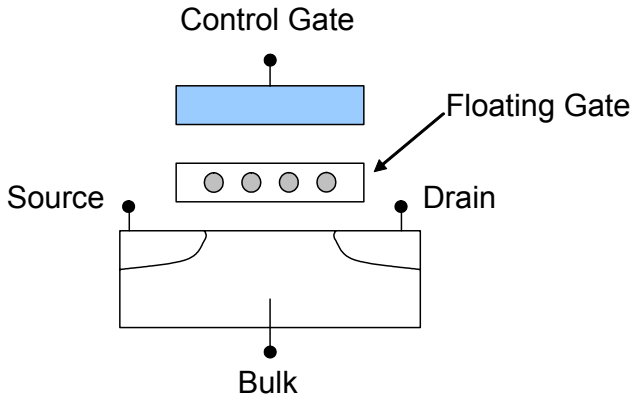
There are several projects included with the Model 4200-FLASH package directed at the testing of floating gate transistors. The package consists of two Model 4205-PG2 cards (four pulse channels), the projects listed here, and all of the required interconnecting cables and adapters. Depending on the desired setup, at least two SMUs are also required. For the most flexibility, the figures below show four SMUs, which permits independent source and measure for each terminal in a typical 4-terminal floating gate transistor.

Theory of operation

Programming and erasing flash memory

A floating gate transistor is just a modified field-effect transistor, with an additional floating gate. The floating gate transistor is the basic structure to store data for non-volatile memory. The floating gate stores charge, which represents the data in the memory (see Figure 1).

Figure 1
Cross section of a floating gate transistor, with stored charge shown in the floating gate



The tests for Flash transistors consist of two parts: 1) Pulse waveforms to program or erase the DUT; 2) DC measurement to determine the state of the device. This implies switching between two conditions: the first where the pulse resources are connected to the DUT, then a second condition where the pulse resources are disconnected and the DC resources are connected to the DUT.

The flash projects support two methods for performing the switching between the pulse and measure phases of the typical flash memory test. The first is the typical method, using a switch matrix to route the pulse or DC signals to the DUT (see Figure 2). Using the switch matrix is more complicated, but provides flexibility for certain tests and test structures that use arrays. Because

both the SMUs and the Model 4205-PG2s have isolation relays located on the cards, it is possible to configure a simpler setup without the external switch matrix (see Figure 3).

To determine the state of the device, one would typically perform a Vg-Id sweep, then utilize a calculation to find the voltage threshold, V_T. The shift in V_T represents a change in the amount of charge stored in the floating gate, which indicates the state of the cell, from fully programmed (1) to fully erased (0). The Model 4200-FLASH package does not include the ability to measure the pulse waveform or pulse response.

Figure 2
Block diagram of an example flash test setup using a switch matrix

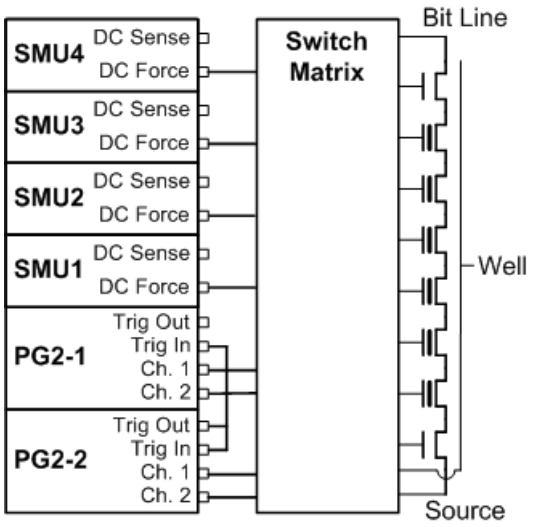
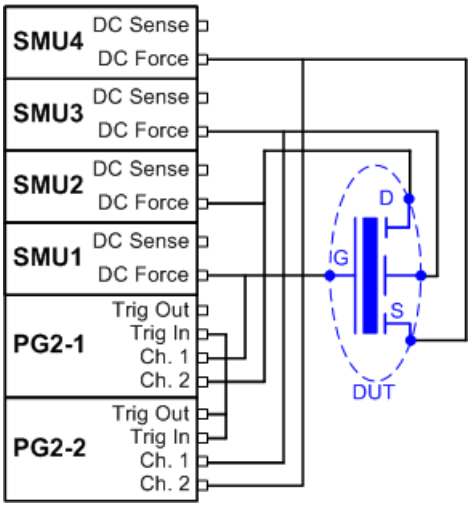


Figure 3
Block diagram of a flash test setup without using a switch matrix



The pulse waveforms are typically a program pulse (see Figure 4), an erase pulse (see Figure 5), or a waveform made up of both program and erase pulses (see Figure 6). All of these waveforms are implemented by using the Segment-Arb capability (see Section 11 of the Model 4200-SCS

Reference Manual). Note that there are many different methods for programming and erasing, so these are just examples.

Figure 4
Example program pulse waveforms for a floating gate DUT, with separate pulse waveforms for the DUT gate, drain, source, and bulk

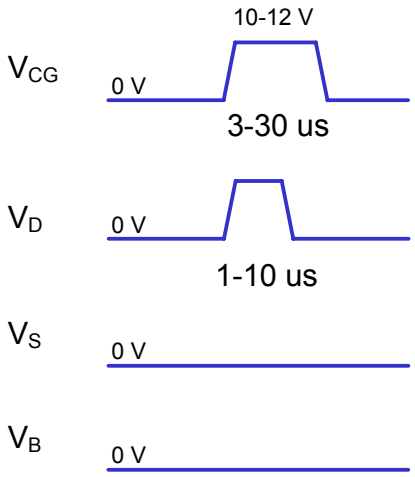


Figure 5
Example erase pulse waveforms for a floating gate DUT, with separate pulse waveforms for the DUT gate, drain, source, and bulk

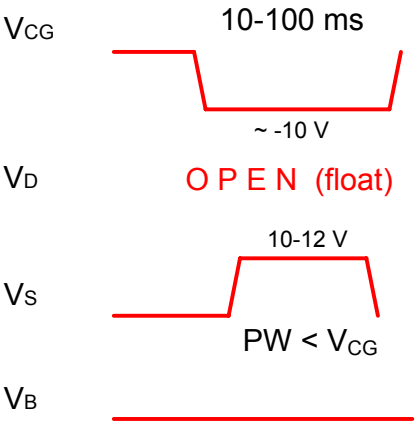
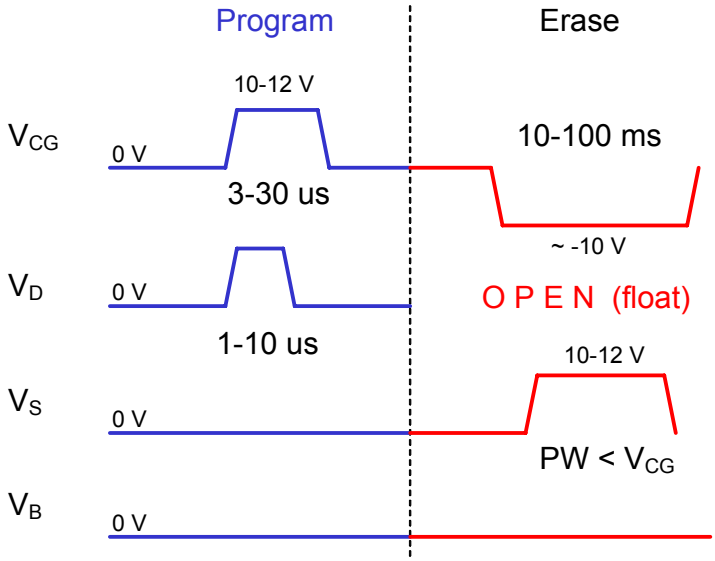
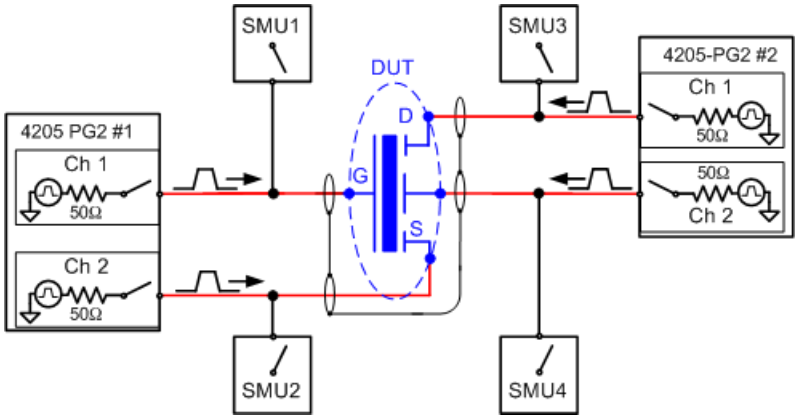


Figure 6
Example Program + Erase pulse waveforms for a floating gate DUT, with separate pulse waveforms for the DUT gate, drain, source, and bulk.



The block diagram for the FLASH setup is shown in Figure 7. Reconfiguring from the pulse stress to DC measure phases is done by activating the switches on the SMU and PG2 cards. During the pulse program/erase phase, the relays in the PG2 channels are closed and the relays in the SMUs are open. For the DC measure phase, the opposite is true.

Figure 7
Basic schematic of Flash testing, without switch matrix



Endurance testing

Endurance testing stresses the DUT with a number of Program+Erase waveform cycles, then periodically measures the V_T. The purpose of these tests is to determine the lifetime of the DUT, based on the number of Program+Erase cycles withstood by the device before a certain amount of shift, or degradation, in the V_T or other measurement.

Disturb testing

The purpose of the Disturb test is to pulse stress a device in an array test structure, then perform a measurement, such as V_T, on a device adjacent to the pulsed device. The goal is to measure the amount of V_T shift in adjacent cells, either in the programmed or erased states, when a nearby device is pulsed with either a Program, Erase, or Program+Erase waveforms. The typical measurement is a V_T extraction based on a Vg-Id sweep, but any type of DC test may be configured.

Figure 8 shows an example configuration to pulse stress a device (Cell 2) and then test an adjacent device (Cell 1) in an array cell memory structure. The solid-line blue circle indicates the cell to be pulse stressed, and the dotted-line red circles are the adjacent memory cells that will be “disturbed” by the stressing. The stress/measure process is explained as follows

Initial test conditions – SMU4 outputs a DC voltage to turn on the control devices for the array. This connects instrumentation at the top of array to the flash memory cells. SMU 2 and SMU3 are set to output 0V. This ensures that only the Cell 2 will be turned on during pulse stressing.

Pulse stressing – The output relay for SMU1 is opened, and the gate and drain of Cell 2 are pulse stressed by PG2 #1 (ch 1) and PG2 #2 (ch 1).

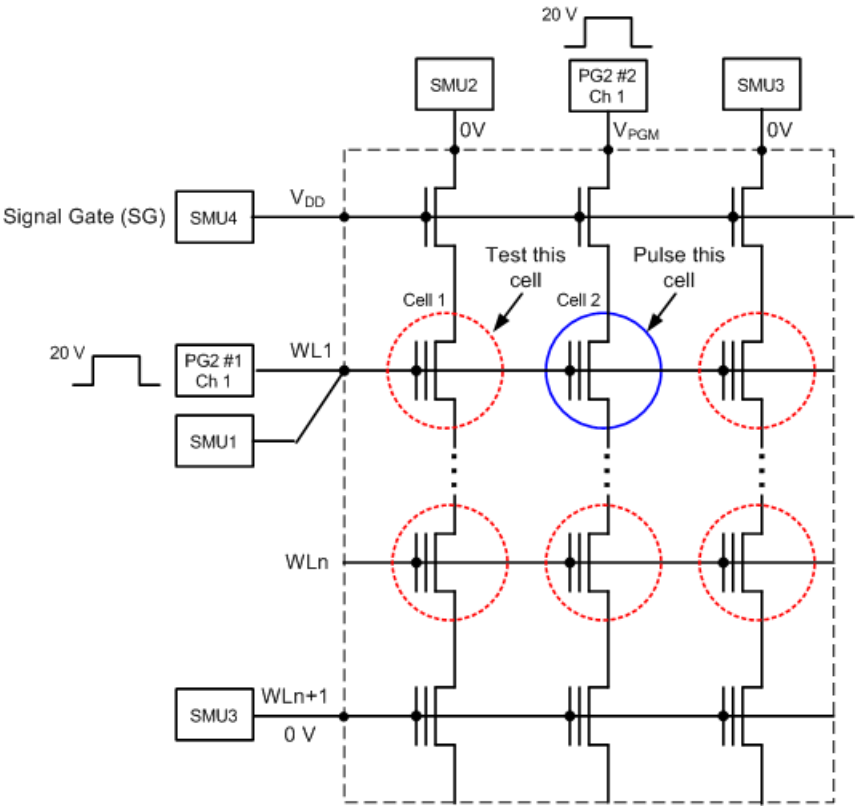
Disturbed cell testing – The outputs for the PG2s are turned off and their output relays for are opened. SMU1 and SMU2 are then used to perform a DC Vg-Vd sweep on Cell 1.

Using a switch matrix

A limitation of the test configuration shown Figure 8 is that only two devices (Cells 1 and 3) can be tested. The test would have to be manually reconfigured to test other devices. Without a switch matrix, the number of adjacent cells that can be measured is limited. Therefore, it is recommended that a switch matrix be used for disturb testing.

Using a switch matrix allows the flexibility of routing pulse and dc signals without having to make connection changes. Also, this type of structure uses a multi-pin probe card, which provides an additional opportunity for mapping test resources to DUT pins. For example, a SMU can be shared where the voltage is the same.

Figure 8
Disturb testing – configuration to test a single device



Connections

The Flash package includes all the necessary cables and adapters required for the test connections. Also included is a an 8in/lb torque wrench for tightening the SMA connections. Figure 10 shows the items that are supplied with the Flash package

Interconnect diagrams for flash testing are shown in Figure 9 and Figure 10. Figure 9 shows the connections for test configuration shown in Figure 7, which is used for program/erase and endurance testing.

Figure 10 shows the connections for test configuration shown in Figure 8, which is used for disturb testing.

Figure 9
Flash connections – program/erase and endurance testing

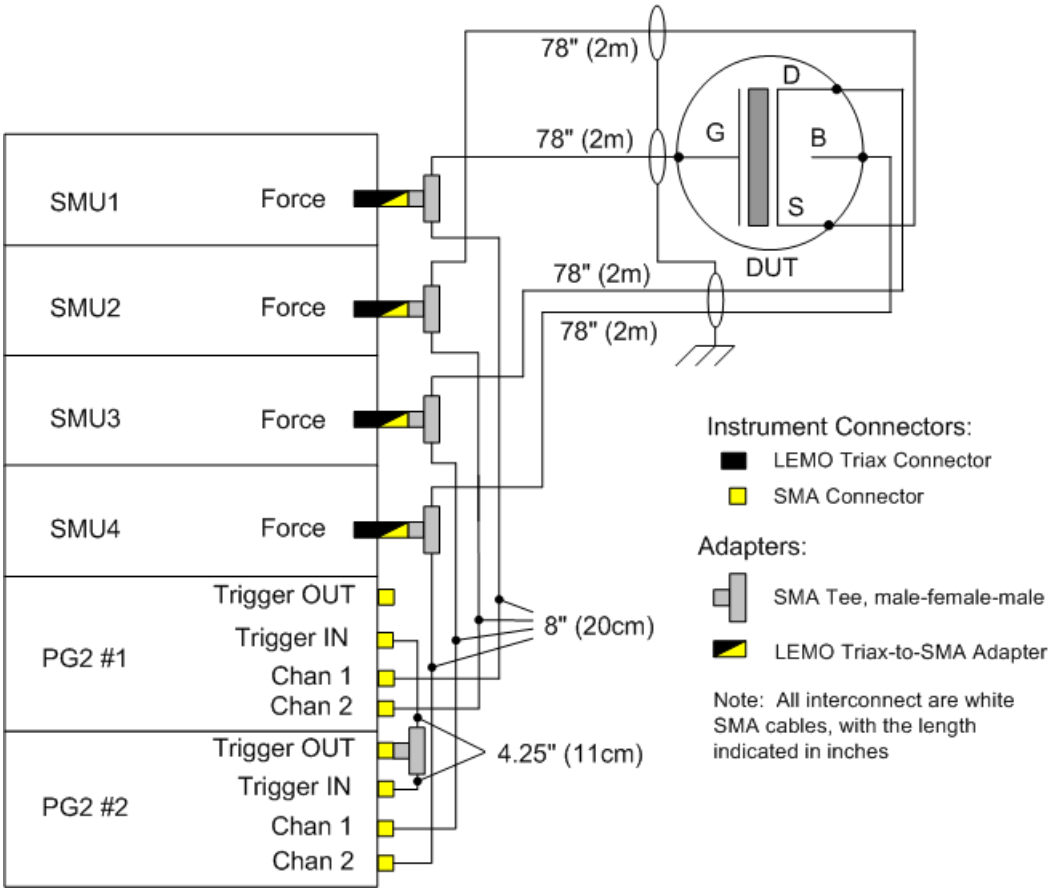


Figure 10
Flash connections – disturb testing

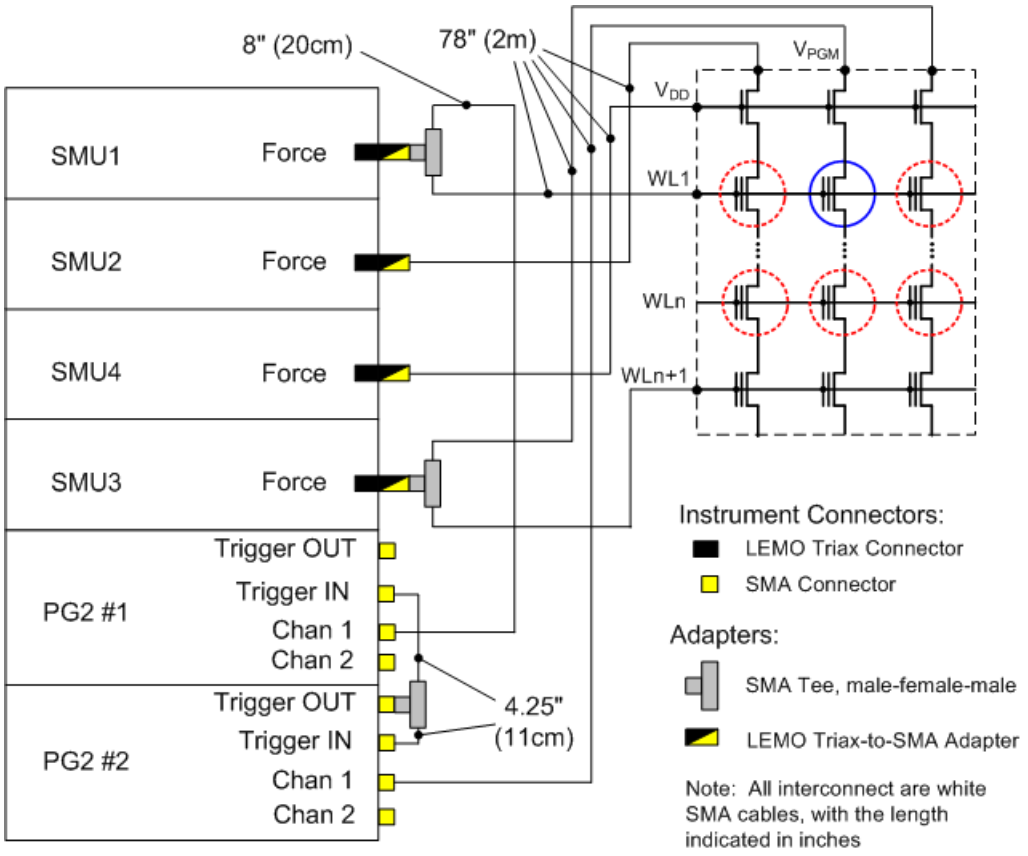
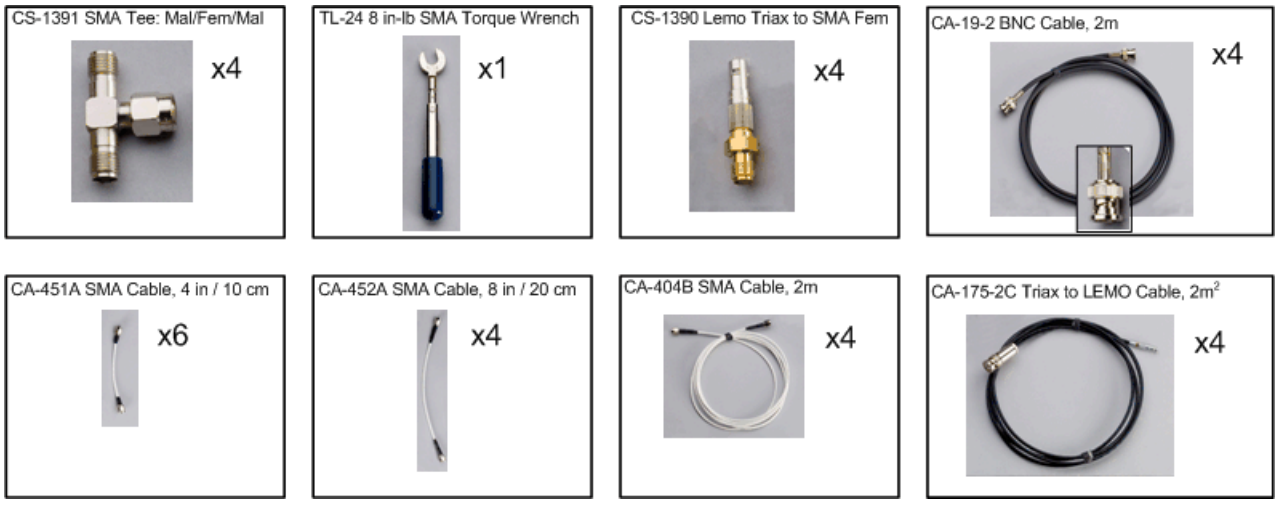


Figure 11
Supplied items for 4200-Flash package



Flash tests

Flash-NAND project
Flash-NOR project
Flash-switch project

These three projects are similar, providing the ability to send n pulses to the DUT, then perform a V_T sweep. These tests allow investigation into program and erase state dependencies on pulse parameters. There are three different waveform types available: Program, Erase, Fast Program and Erase. The Program waveform and Erase waveform output pulses with a single set of parameters for the pulse width, transition and level. The Fast Program and Erase waveform uses two pulses, which can have independent widths and levels. Each test permits programming the pulse width, level and transition (rise/fall) parameters, as well as the number of pulses. For extended Program Erase cycling, use one of the FlashEndurance projects. Instead of a voltage, note that the disconnected, or open, state may also be chosen for any pulse. The open state is useful when using CHEI (channel hot electron injection) for programming or erasing a floating gate transistor.

These projects support both 4-terminal and 8-terminal testing. Note that the 8-terminal testing requires four Model 4205-PG2 cards and, for most tests, an external switch matrix.

The purpose of these projects is to initially characterize a floating gate transistor. For example, determining the appropriate pulse parameters for both the program and erase waveforms to reach a target Vt_{erase} and Vt_{prog}. This can be done by setting the Program pulse height to the desired value, but setting the pulse width to a fraction of the expected pulse width. Set the NumPulses to 1 and uncheck the Erase and Fast-Program-Erase tests. Run through the Program, SetupDC and Vt-MaxGm tests, monitoring the shift in the Vt and noting the number of pulses required to reach the target Vt_{prog}. Then the same approach can be used for the erase. If the DUT was initially in an unknown state, the determination of appropriate pulse parameters for the program and erase waveforms may be iterative. The Fast-Program-Erase test may be used to confirm that the chosen pulse parameters are providing a acceptable erase and that the Vt after the Fast-Program-Erase is not shifting. Once acceptable pulse parameters are determined, use Kpulse to define and save the waveforms for use in the Endurance and Disturb projects.

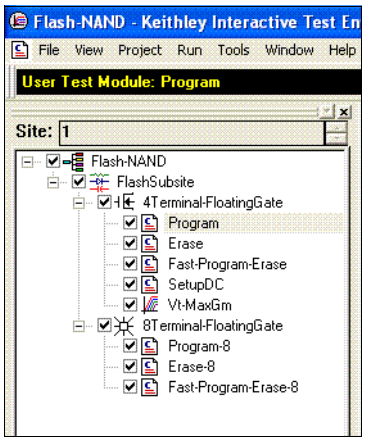
The difference between the Flash-NAND and Flash-NOR are the typical pulse widths and levels specific to the DUT type. The Flash-switch is a generic example of the Flash testing described above, but adds support for an external Keithley switch matrix.

Flash-NAND tests

Program
Erase
Fast-Program-Erase
SetupDC
Vt-MaxGm
Program-8
Erase-8
Fast-Program-Erase-8

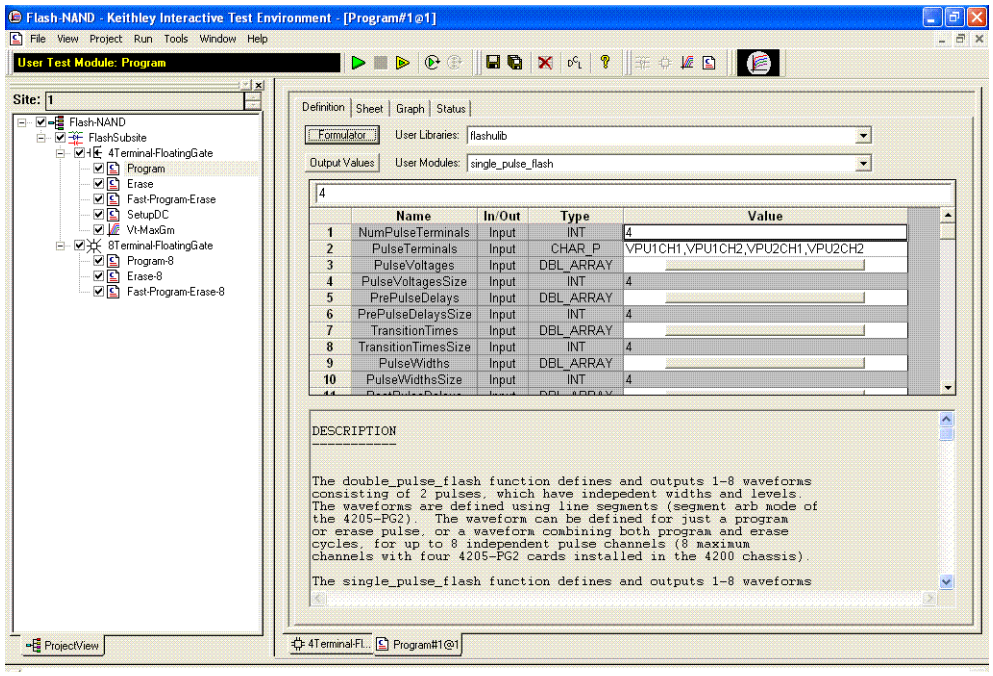
The Flash-NAND project plan is shown in Figure 12.

Figure 12
Flash-NAND project plan



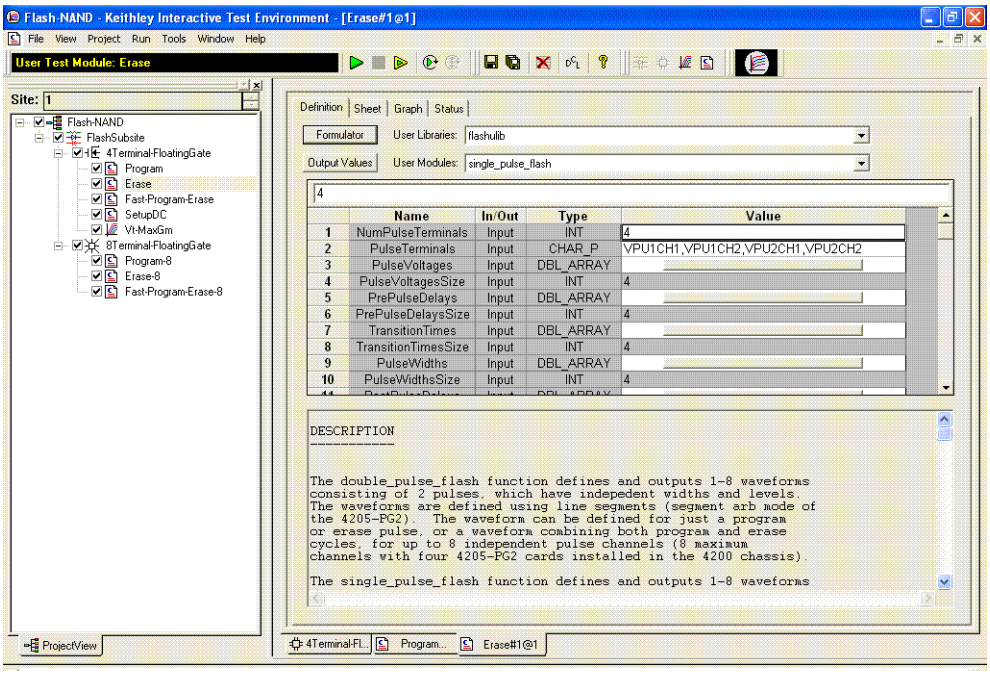
Program test – This test uses Segment Arb waveforms to program a flash memory device. The Definition tab for this test is shown in Figure 13.

Figure 13
Flash-NAND project – Program definition tab



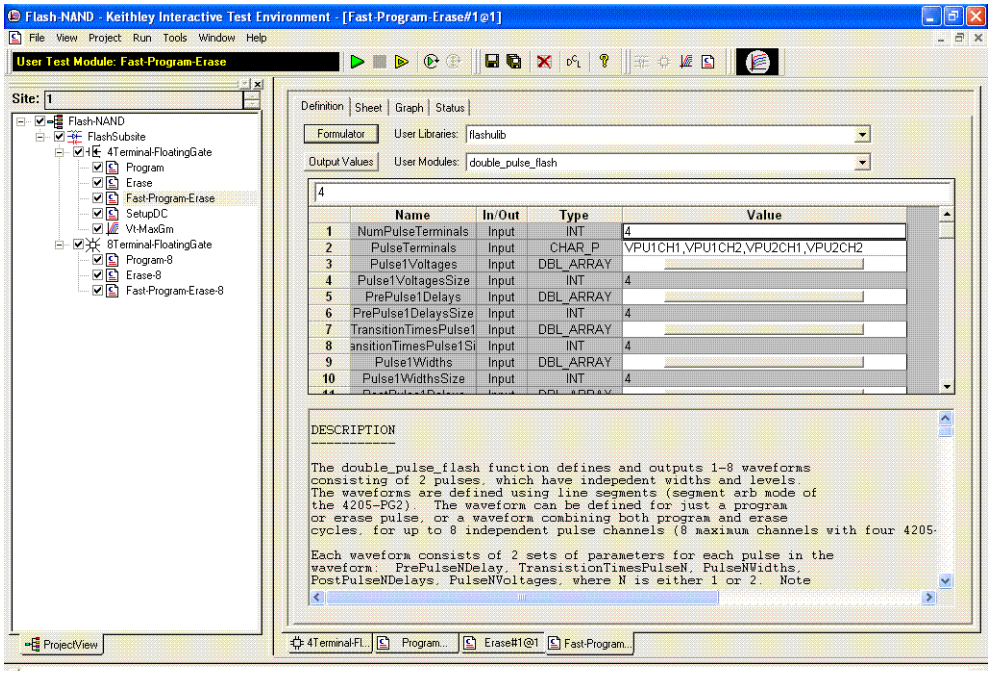
Erase test – This test uses predefined Segment Arb waveforms to erase a flash memory device. The Definition tab for this test is shown in Figure 14.

Figure 14
Flash-NAND project – Erase definition tab



Fast-Program-Erase test – This test uses predefined Segment Arb waveforms to program and erase a flash memory device. The Definition tab for this test is shown in Figure 15

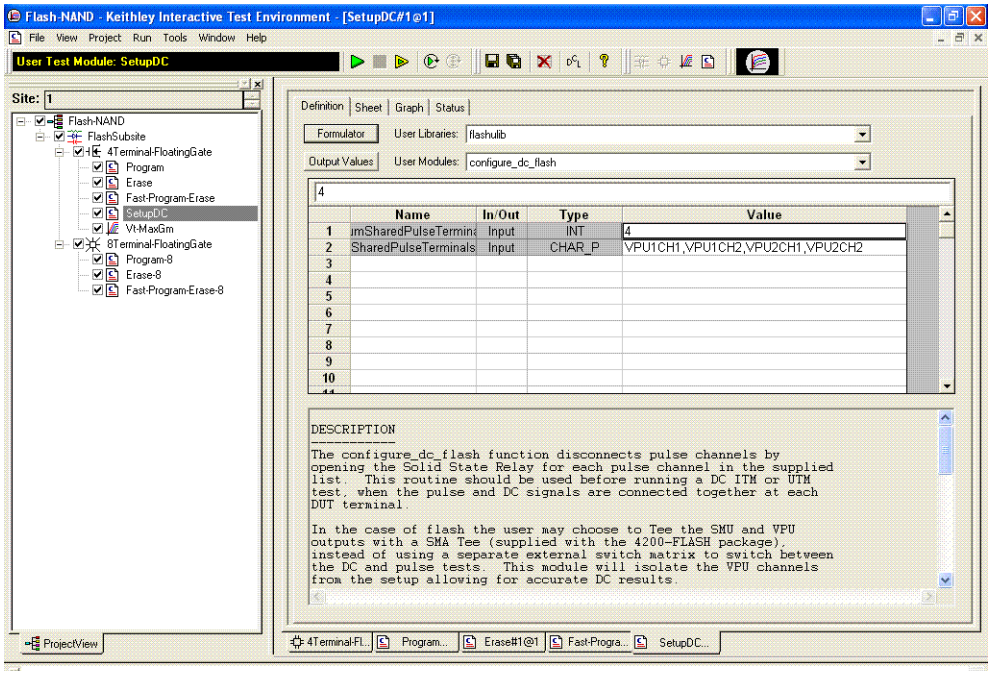
Figure 15
Flash-NAND project – Fast-Program-Erase definition tab



SetupDC test – The Definition tab for this test is shown in Figure 16. This test isolates the VPU outputs from the DUT. It does this by opening the High Endurance Output Relay for each VPU channel. Disconnecting the VPU channels allows for accurate DC results.

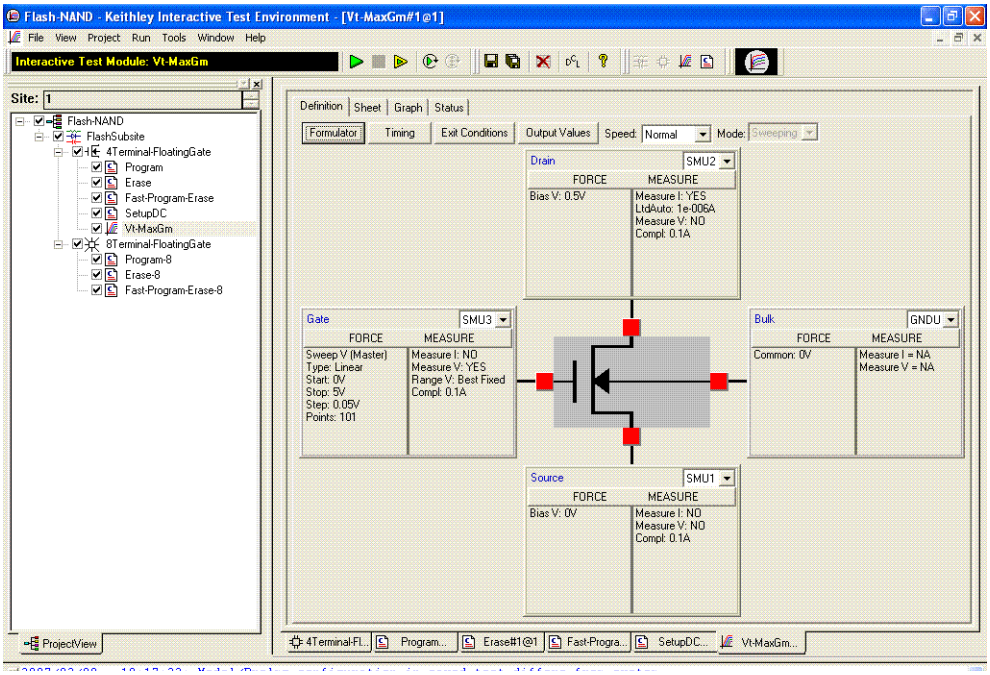
The SetupDC test step is used in the configuration without a switch matrix and is required before any DC tests. When using a switch matrix, a ConPin test is used (see the `config` LPT function in Section 8 of the Reference Manual) to set the appropriate matrix connections prior to any DC tests.

Figure 16
Flash-NAND project – SetupDC definition tab



Vt-MaxGm test – This test is used to perform a DC voltage sweep on the gate of the DUT and measure the drain current at each sweep step. The default Definition tab for this test is shown in Figure 17. SMU3 is configured to perform a 101 point sweep from 0 to 5V in 50mV steps. SMU1 is configured to DC bias the drain at 0.5V and measure current at each step of the sweep.

Figure 17
Flash-NAND project – Vt-MaxGm definition tab



Program-8 test – This test uses Segment Arb waveforms to program an 8-terminal flash memory device.

Erase-8 test – This test uses Segment Arb waveforms to erase an 8-terminal flash memory device.

Fast-Program-Erase-8 test – This test uses Segment Arb waveforms to program and erase an 8-terminal flash memory device.

Flash-NOR tests

The Flash-NOR project has tests similar to the Flash-NAND project, with defaults for NOR type floating gate DUTs.

Flash-switch tests

The Flash-Switch project has similar tests to the Flash-NAND, with defaults for using a switch matrix for more complex multi-DUT addressable test structures (see Figure 2).

FlashEndurance-NAND project
FlashEndurance-NOR project
FlashEndurance-switch project

These three projects are similar and stress the DUT with a number of Program+Erase waveform cycles, then periodically measures the V_T. The purpose of these projects is to determine the lifetime of the DUT, based on the number of Program+Erase cycles withstood by the device before a certain amount of shift, or degradation, in the V_T or other measurement. The waveforms may be unique for each pulse channel, and are defined in the separate Kpulse program (see Section 13 of the Model 4200-SCS Reference Manual) and saved to files. These files are specified for each pulse channel in the test. The number and interval for the pulse stresses are set, as well as the desired SMU measurements. The typical measurement is a V_T extraction based on a Vg-Id sweep, but any type of DC test may be configured.

The difference between the FlashEndurance-NAND and FlashEndurance-NOR are the difference in the typical pulse widths and levels specific to the DUT type. The FlashEndurance-switch is a generic example of the Flash testing described above, but adds support for an external Keithley switch matrix. Example results for the Endurance tests are shown in Figure 21.

FlashEndurance-NAND tests

Program
SetupDC-Program
Vt-MaxGm-Program
Erase
SetupDC-Erase
Vt-MaxGm-Erase

The project plan for FlashEndurance-NAND is shown in Figure 18. Stressing for the FlashEndurance-NAND tests are configured from the Subsite Setup tab for the FlashEndurance subsite plan. The default setup (shown in Figure 19) uses Segment Arb waveforms to perform log stressing that ranges from 1 to 100,000 counts.

The Segment Arb waveform files (Flash-NAND-Vg-ksf and Flash-NAND-Vd-ksf) used for stressing are loaded into the Device Stress Properties window shown in Figure 20. The stress properties window is opened by clicking the **Device Stress Properties** button in Figure 19. Example results for the Endurance tests are shown in Subsite Graph tab (see Figure 21).

Figure 18
FlashEndurance-NAND project plan

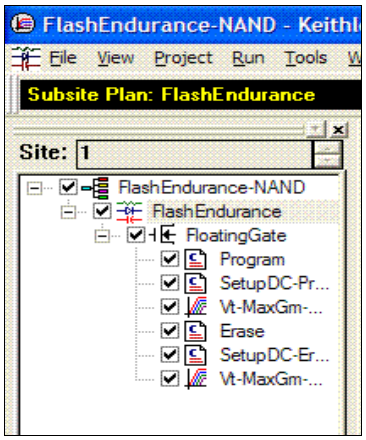


Figure 19
FlashEndurance-NAND project – Subsite Plan tab

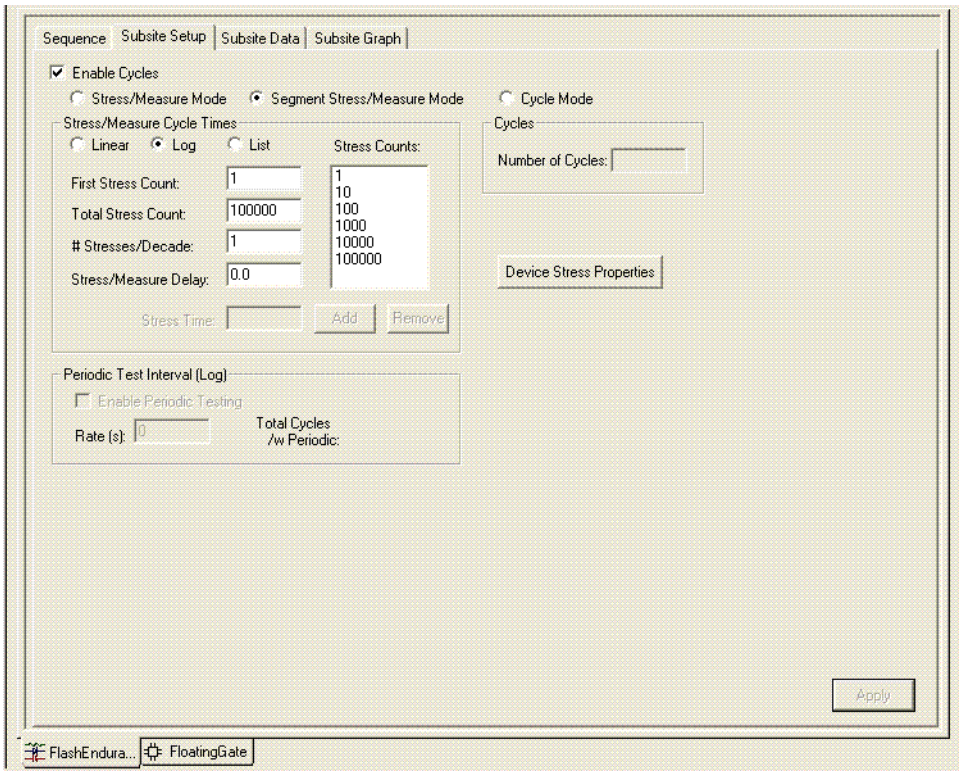


Figure 20
FlashEndurance-NAND project – Device Stress Properties

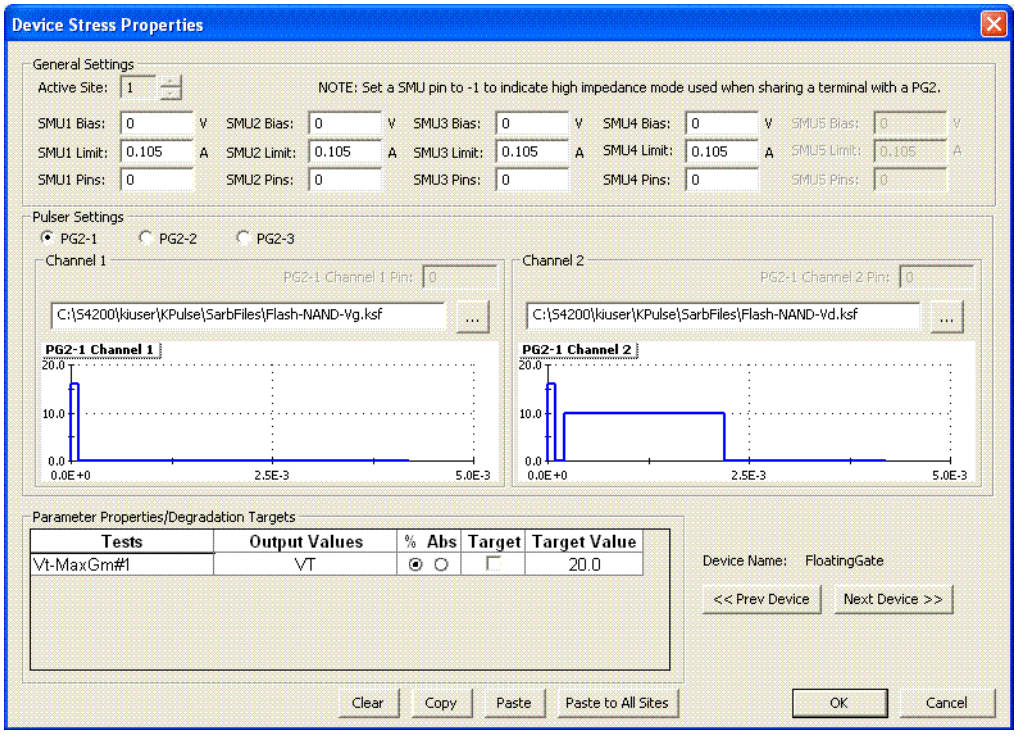
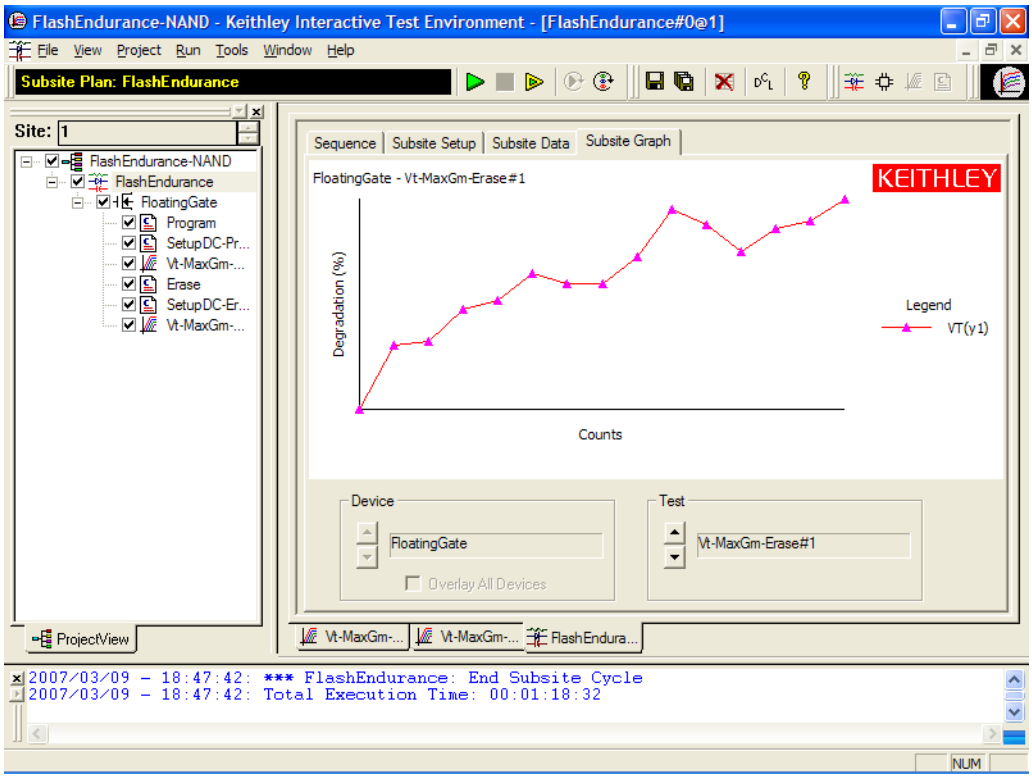
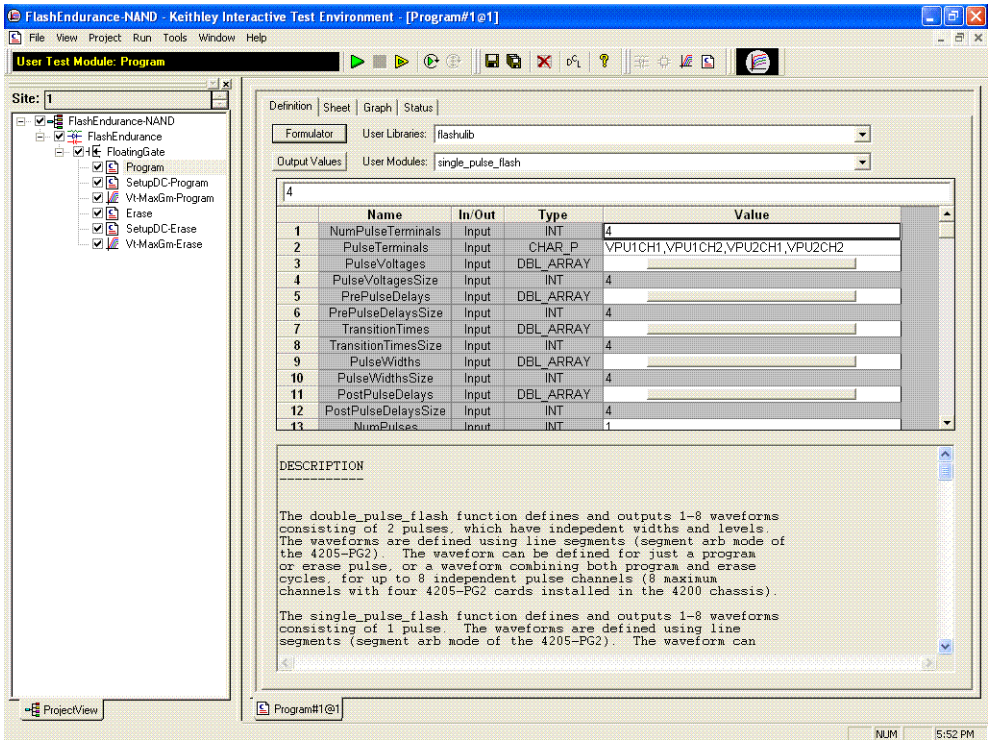


Figure 21
FlashEndurance-NAND project – Subsite Graph tab



Program test – The Definition tab for this test is shown in Figure 22. This test uses Segment Arb waveforms to program a flash memory device.

Figure 22
FlashEndurance-NAND project – Program Definition tab

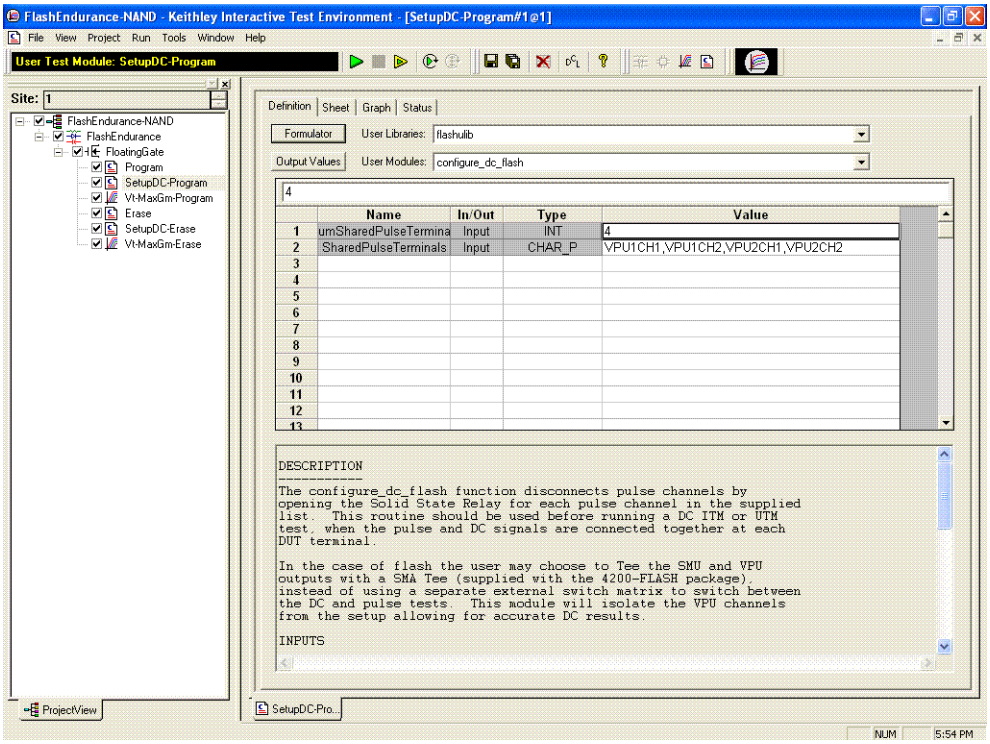


SetupDC-Program test – The Definition tab for this test is shown in Figure 23. This test isolates the VPU outputs from the DUT. It does this by opening the High Endurance Output Relay for each VPU channel. Disconnecting the VPU channels allows for accurate DC results.

The SetupDC test is a UTM that should be used when using a directly wired DUT, without an external switch matrix. SetupDC disconnects the PG2 channels from the DUT to permit proper operation of any subsequent DC measurements.

When using a switch matrix, a ConPin test is used (see the `config` LPT function in Section 8 of the Reference Manual) to set the appropriate matrix connections prior to any DC tests.

Figure 23
FlashEndurance-NAND project – SetupDC Definition tab



Vt-MaxGm-Program test – This test is used to perform a DC voltage sweep on the gate of the DUT and measure the drain current at each sweep step. The default Definition tab for this test is shown in Figure 24. SMU3 is configured to perform a 101 point sweep from 0 to 5V in 50mV steps. SMU1 is configured to DC bias the drain at 0.5V and measure current at each step of the sweep. The results of the test are shown in the Graph tab (Figure 25).

The Vt-MaxGm tests may be replaced with another Vt or DC test. Or, additional DC tests may be added after this test.

Figure 24
FlashEndurance-NAND project – Vt-MaxGm-Program Definition tab

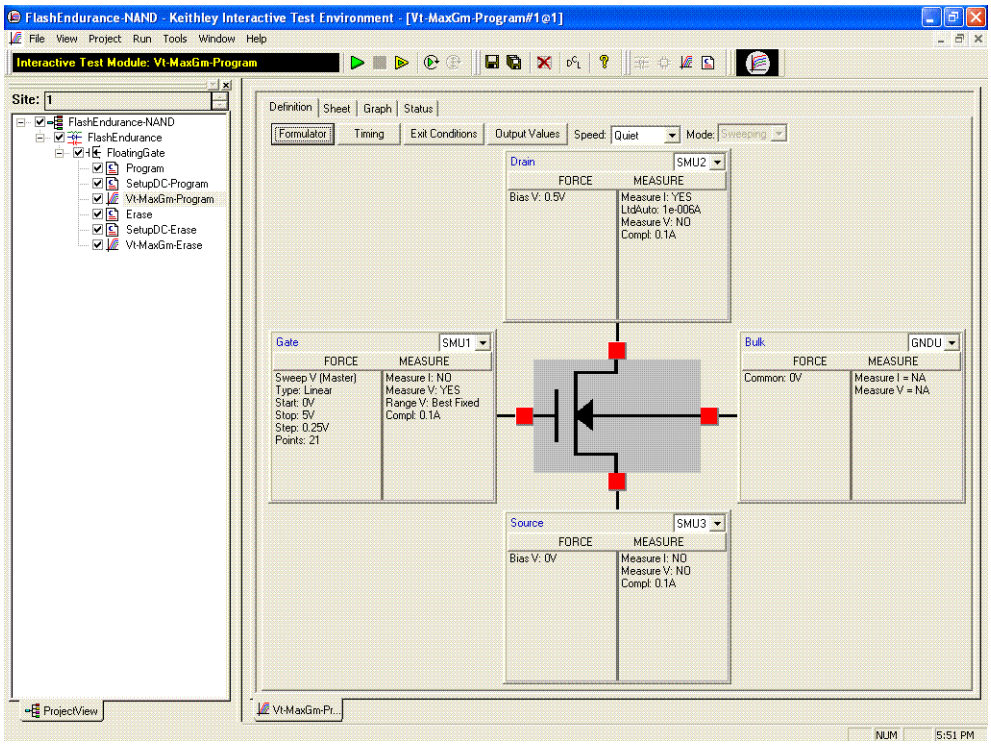
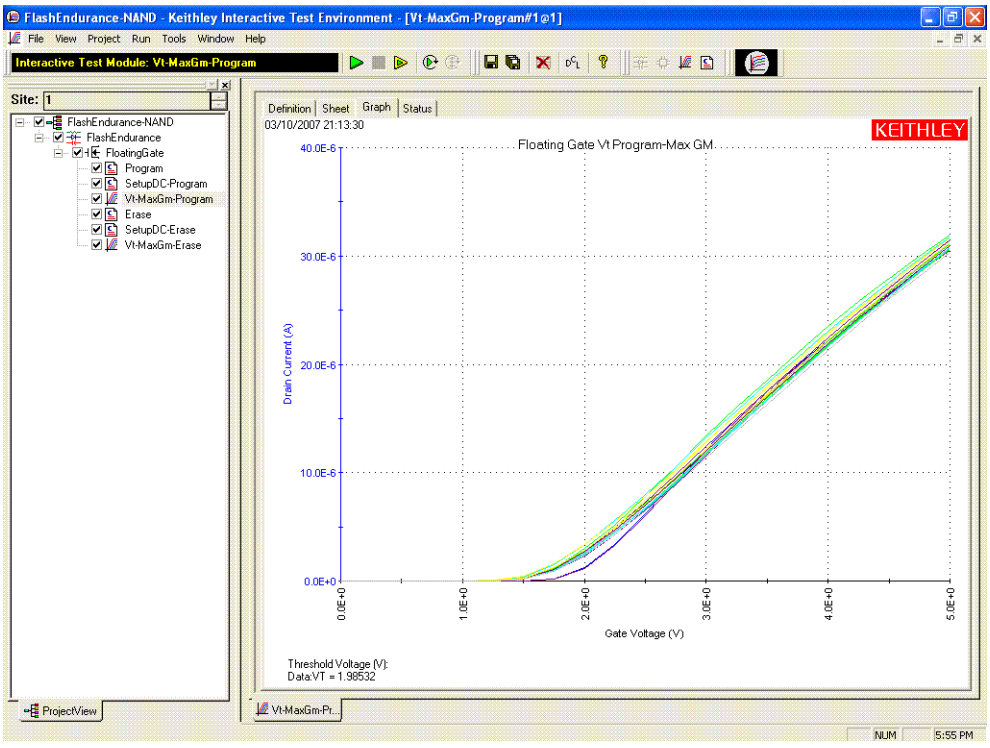
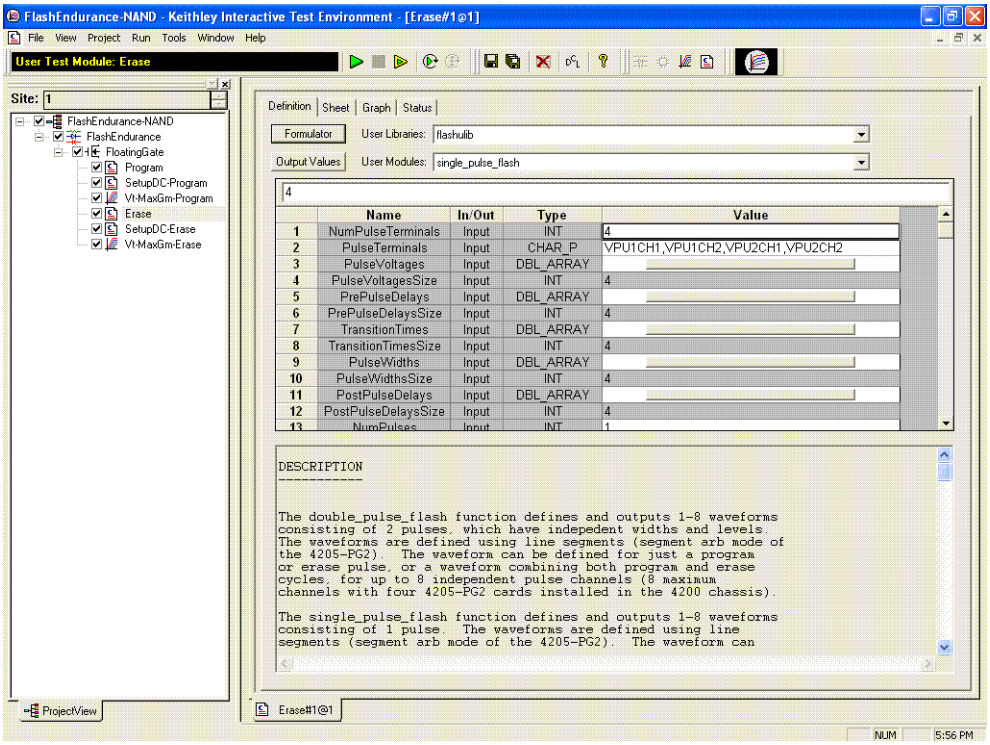


Figure 25
FlashEndurance-NAND project – Vt-MaxGm-Program Graph tab



Erase test – This test uses Segment Arb waveforms to program a flash memory device. The default Definition tab for this test is shown in Figure 26.

Figure 26
FlashEndurance-NAND project – Erase Definition tab



SetupDC-Erase test – This test isolates the VPU outputs from the DUT. It does this by opening the High Endurance Output Relay for each VPU channel. Disconnecting the VPU channels allows for accurate DC results.

Vt-MaxGm-Erase test – This test is used to perform a DC voltage sweep on the gate of the DUT and measure the drain current at each sweep step. SMU3 is configured to perform a 101 point sweep from 0 to 5V in 50mV steps. SMU1 is configured to DC bias the drain at 0.5V and measure current at each step of the sweep.

The Vt-MaxGm tests may be replaced with another Vt or DC test. Or, additional DC tests may be added after this test.

FlashEndurance-NOR tests

The FlashEndurance-NOR project has tests similar to the FlashEndurance-NAND project, with defaults for NOR type floating gate DUTs.

FlashEndurance-switch tests

The FlashEndurance-switch project has similar tests to the FlashEndurance -NAND, with defaults for using a switch matrix for more complex multi-DUT addressable test structures (see Figure 2).

FlashDisturb-NAND project
FlashDisturb-NOR project
FlashDisturb-switch project

These three projects are similar and use the shared stress-measure looping capability of the FlashEndurance projects. The purpose of the Disturb test is to pulse stress a device in an array test structure, then perform a measurement, such as V_T, on a device adjacent to the pulsed device. The goal is to measure the amount of V_T shift in adjacent cells, either in the programmed or erased states, when a nearby device is pulsed with either a Program, Erase, or Program+Erase waveforms. The typical measurement is a V_T extraction based on a Vg-Id sweep, but any type of DC test may be configured.

The difference between the FlashDisturb-NAND and FlashDisturb-NOR are the typical pulse widths and levels specific to the DUT type. The FlashDisturb-switch is a generic example of the Flash testing described above, but adds support for an external Keithley switch matrix.

FlashDisturb tests

Program
SetupDC-Program
Vt-MaxGm-Program
Erase
SetupDC-Erase
Vt-MaxGm-Erase

The six tests listed above are the same ones used for endurance testing (see "FlashEndurance-NAND tests" for details).

Stressing for the disturb tests are configured from the Subsite Setup tab for a disturb project subsite plan. The default subsite setup for FlashDisturb-NAND (shown in Figure 27) uses Segment Arb waveforms, defined and saved to file using Kpulse, to perform log stressing that ranges from 100,000 to 1,000,000 counts.

The Segment Arb waveform files (Flash-NAND-Vg.ksf and Flash-NAND-Vd.ksf) used for stressing are loaded into the Device Stress Properties window shown in Figure 28. The stress properties window is opened by clicking the **Device Stress Properties** button in Figure 27.

Figure 27
FlashDisturb-NAND project – Subsite Setup tab

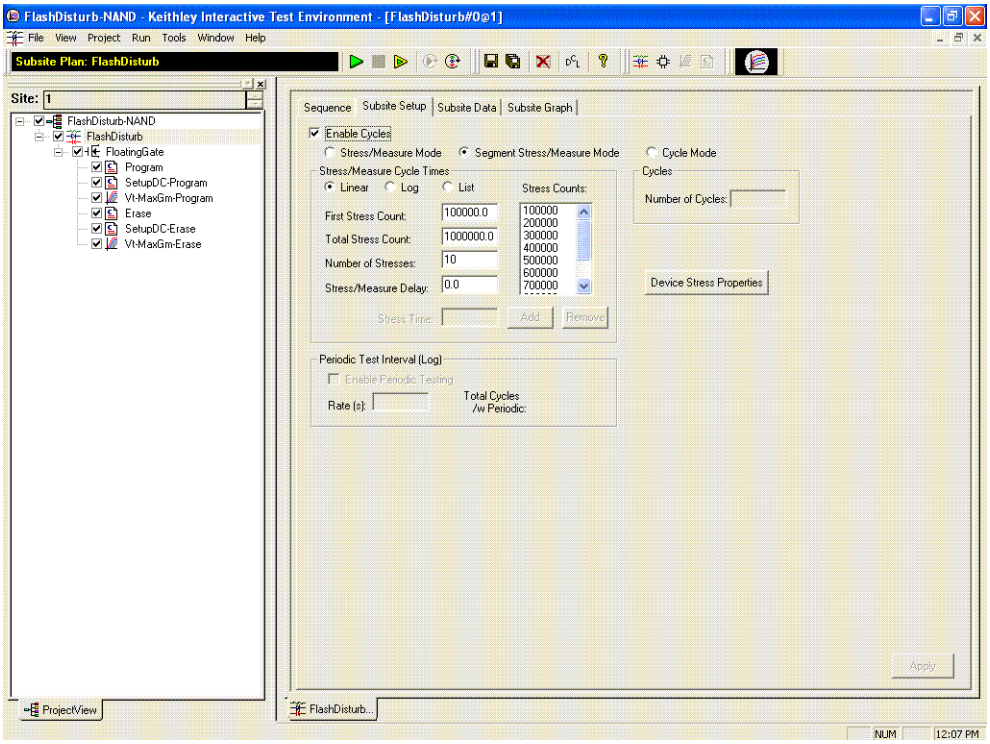


Figure 28
FlashDisturp-NAND project – Device Stress Properties