**Keithley Instruments, Inc.**
28775 Aurora Road
Cleveland, Ohio 44139
1-888-KEITHLEY
www.keithley.com

# Model 4200-PIV-Q Pulse IV Measurements for Compound Semiconductor and LDMOS Transistors

## What is Pulse IV?

Pulse IV provides a user with the capability of running parametric curves on devices using pulsed rather than DC signals. Pulse IV is basically considered a pulse source with a corresponding pulse measurement and can be used in two general ways.

The first method is to provide DC-like parametric tests, where the measurement happens during the flat, settled part of the pulse. Typical tests are IV sweeps, such as a $V_D$-$I_D$ family of curves or a $V_G$-$I_D$ curve used for $V_T$ extraction.

The second method is transient testing, where a single pulse waveform is used to investigate time-varying parameter(s). An example of this second case would be using a single pulse waveform to investigate the $I_D$ degradation versus time due to charge trapping or self-heating.

In both cases, using a low duty cycle pulse waveform, typically around 1% or less is used to minimize the energy dissipated in the device under test.

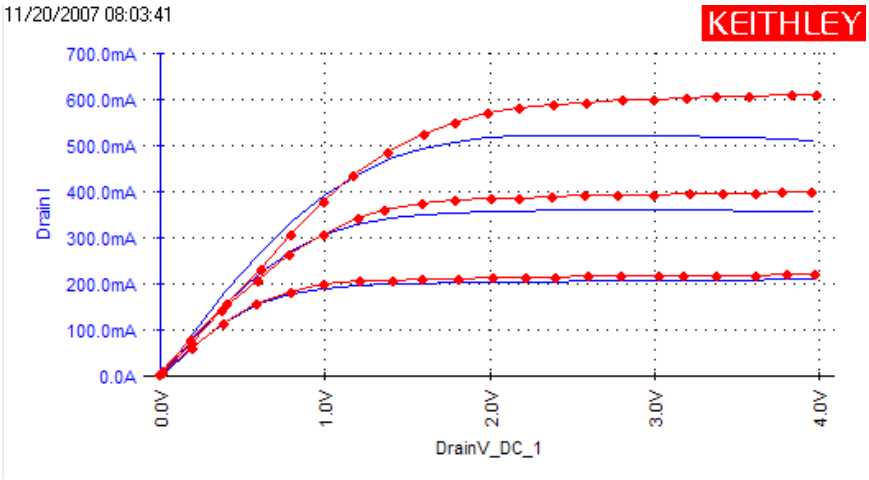


**Figure a.** Vd-Id curve showing device self-heating on the blue DC curve and corresponding pulse IV curve (red, dotted) without self-heating.

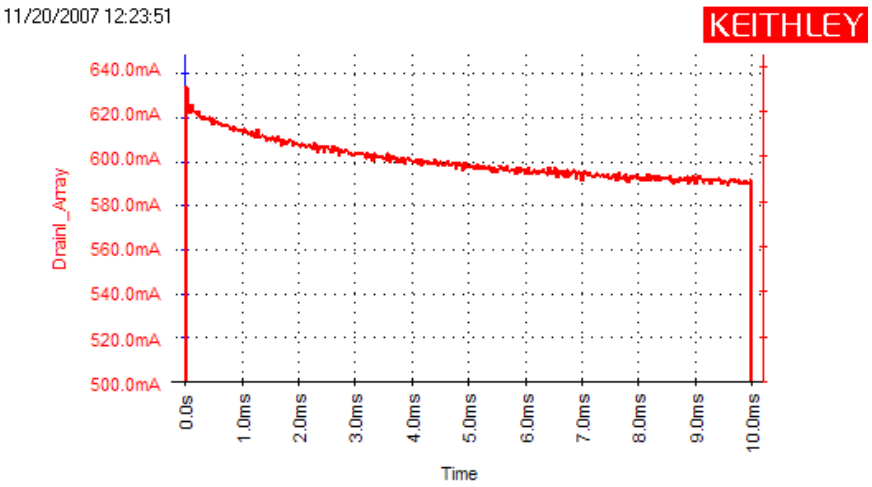


**Figure b.** Single pulse graph showing device self-heating versus time. Note $I_D$ starts at 630 mA and declines to 590 mA over a 10 ms pulse width.

## What is Q-point Pulse IV?

Q-point Pulse IV is a method that sources pulses with a non-zero base or offset. The "Q" refers to quiescent or bias level, which puts the transistor device under test (DUT) into an appropriate operational state. This means that the DUT is partially "on" or conducting in between each test pulse. In addition to bias point or Q point terminology; this approach is sometimes called pulsing from an operating point.

Q- or bias-point operation is typically used for RF transistors in amplification or switching applications. Of course, if a non-zero bias point is not required, the system can be used with zero settings for the pulse offset. Using 0V instead of non-zero values allows the 4200-PIV-Q system to be used as a general purpose voltage pulsing pulse IV measurement system useful for a wide variety of devices.

## Why use Q-point Pulse IV?

Using a non-zero bias point determines its overall response of the DUT. For example, a transistor used in switching applications will switch faster if the transistor is slightly on or conducting, than if it was completely turned off. Using a Q-point approach, various performance characteristics of transistors used for amplification can be optimized: gain, linearity, battery drain. Since this Q point can have a significant effect on the device performance, and it is the way the device is used in the final application, the characterization instrumentation must be able pulse from a similar non-zero Q point.

Another need for a non-zero base value for the pulse is for testing depletion mode devices. To turn off a depletion mode transistor, a negative voltage is applied to the gate. Pulsing the gate to a less negative voltage, or a positive voltage, begins to turn on the depletion mode transistor.

In general, the values used for the bias point are chosen to balance the performance tradeoffs between many factors, such as standby power or leakage current, amplification, linearization, response speed.

## What is the 4200-PIV-Q Pulse IV Package?

The 4200-PIV-Q package is an optional factory-installed kit for the Keithley 4200-SCS, with all source and measurement hardware contained within the 4200-SCS chassis. The focus for the 4200-PIV-Q package is testing RF transistors that exhibit dispersion. Dispersion is broadly defined as any behavior that causes a difference between DC and Pulse IV characterization and is generally caused by self-heating and charging or charge trapping effects.

To accomplish pulse IV testing of RF FETs, the 4200-PIV-Q package consists of:

- 4205-PG2 Dual channel voltage pulse generator, Qty: 3
- 4205-PCU Module that combines four 4205-PG2 channels into a single, higher power pulse channel
- 4200-SCP2HR Dual channel oscilloscope
- Pulse IV Interconnect Adapters and cables to combine both DC and pulse signals to a single cable for each the DUT gate and drain terminals
- Pulse IV Q software Projects and test routines for testing of RF FETs, including cable compensation and load-line algorithms to provide DC-like sweep results

## Target Applications and Test Projects

The 4200-PIV-Q package includes tests that address the most common parametric transistor tests: Vds-id and Vgs-id for higher power FETs. These tests are provided in both DC and Pulse modes, allowing correlation between the two test methods. For system setup validation and DUT transient testing, there is a scope shot test, which graphs the pulse waveform versus time, based on a single set of test parameters.

These tests, as well as initialization steps for scope auto-calibration and cable compensation, are included in a single 4200 test project, QPulseIV-Complete. A second 4200 project, Demo-QPulseIV, has the same tests, but the parameters are optimized for demonstration of the PIV-Q package using a test fixture and demo DUT (Figure 9).

## Overall 4200-PIV-Q Capabilities

- Pulse voltage on both gate and drain simultaneously for FET (HEMT, LDMOS)
- Non-zero voltage between pulses, also called Q point, or bias point capability
- Pulse widths from 500 ns to 999 ms (FWHM)
- Duty cycles from 0.01 to 99%
- ±20V for Gate (up to 400 mA into 50 Ω)
- ±38V for the Drain (at 760 mA into 50 Ω)*
- Measurements: $V_G$, $I_G$, $V_D$, $I_D$
- $V_D$-$I_D$ (family of curves) and $V_G$-$I_D$ sweeps
- Single pulse scope snapshot for setup validation, oscillation discovery and verification, or transient testing

* See section “Maximum Voltage and Current for the Drain and Gate” and Table 5 for other maximum $V_D$ and $I_D$ values for other $R_{DS}$ impedances.

## Theory of Operation

In general, the PIV-Q package performs Pulse IV testing by synchronously providing pulses to both the gate and drain of the DUT. The source and body connections are connected to ground/shield. The pulse levels for the gate and drain can be between any two voltage levels within the specified capabilities, thus providing bias point or non-zero offset between the pulses. The pulse duty cycles are typically low, around 1% or less, but the system supports higher duty cycles for DC-like tests while still utilizing the pulse source and measure hardware.

The DC IV tests are performed using the SMU hardware, while pulse IV uses the pulse sources and the scope card. Switching the signal path to the DUT between DC IV tests and Pulse IV is accomplished by using switching located on the individual instrument cards (Figure 1) and done when running a DC or Pulse IV test.

The dual channel oscilloscope (4200-SCP2HR) measures the gate voltage and drain voltage. The drain current is calculated by the voltage drop across the 5 Ω sense resistor in the 4205-PCU (Figure 1, 5 Ω sense resistor in 4205-PCU). The gate current is determined by measuring the voltage at the output of the 50 Ω impedance and comparing to the voltage value sourced, with the difference being caused by the voltage drop across the 50 Ω resistor in the PG2.

The 4205-PCU combines 4 pulse output channels of 4205-PG2 into one higher power pulse output channel (Figure 2). This higher powered pulse channel is connected to the DUT drain and provides 38 V into a 50 Ω load (760 mA max). Pulsing into a drain-source resistance different from 50 Ω will provide either higher voltage ($R_{DS}$ > 50 Ω) or higher current ($R_{DS}$ < 50 Ω). See the section "Maximum Voltage and Current for the Drain and Gate" for more information. The DUT gate is pulsed by ±20V from the third 4205-PG2 card (on the left side of Figure 1).

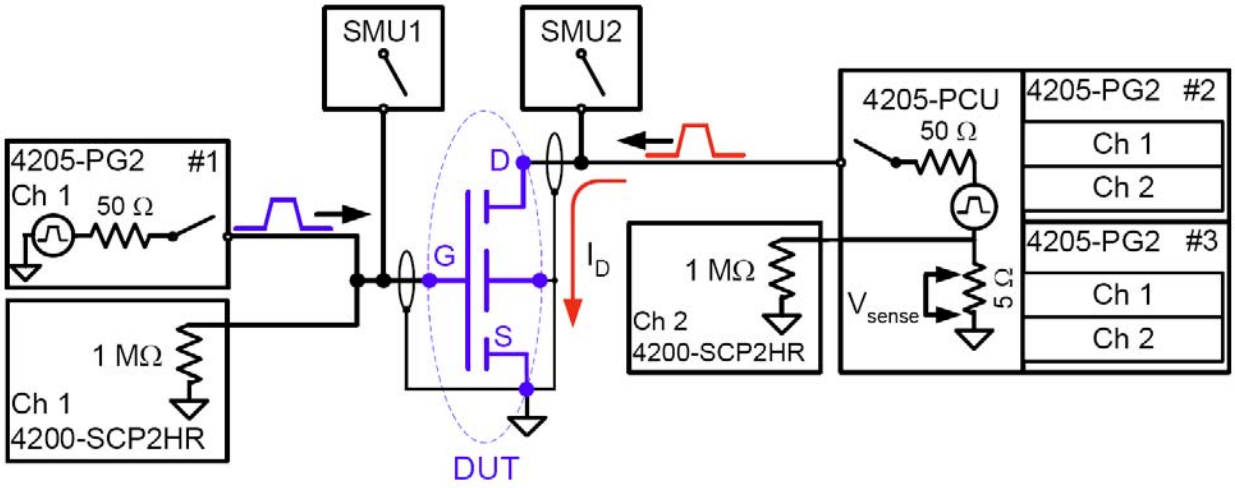


***Figure 1.*** *4200-PIV-Q schematic diagram, with 2 SMUs. When DC testing with the SMUs, the relays in SMU1 and SMU2 are closed, while the relays in 4205-PG2 #1 and 4205-PCU are opened. For pulse IV testing, the SMU relays are opened, while the PG2 and PCU relays are closed.*

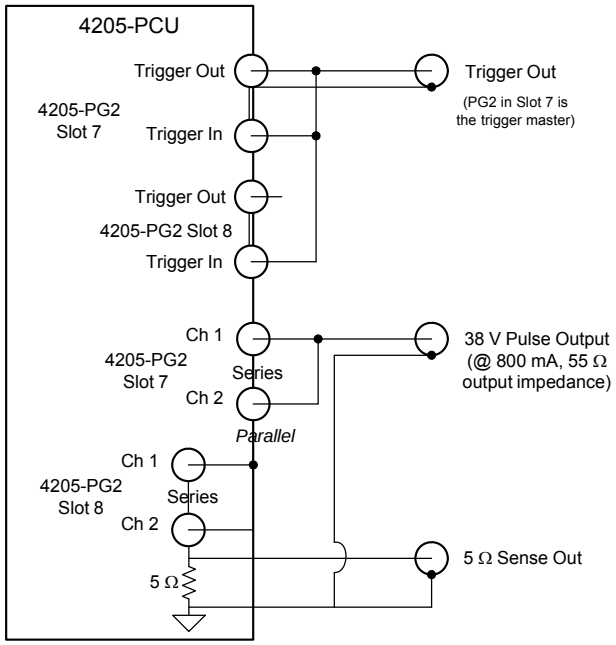


***Figure 2.*** *4205-PCU schematic diagram. The 4205-PCU combines the 4 pulse channels from two pulse cards into one higher power pulse channel to power the DUT drain. It also connects the triggers between the two cards.*

## Load Line Effect and Compensation

The load line effect is a voltage drop across a resistance due to current flow. This effect causes a reduction in the voltage available at the DUT as the current reaches higher values. In general, this is an undesirable effect. It is most commonly seen where a resistor is used to measure current flow through a device, and this current measure method is called a shunt ammeter. Digital multimeters (DMM) use this approach to measure current. The shunt ammeter approach is also used for measuring pulse current signals, because of its straightforward implementation and high bandwidth. For any given current, a larger sense resistor will provide a larger voltage. Using a larger sense resistor provides a larger voltage, which makes measuring the signal easier, especially important for sub-microsecond measurements. The trade-off is that there is a larger voltage drop across this larger sense resistor, which means that the device is getting an even smaller voltage. To overcome this effect, the source voltage is increased, so that the voltage at the device matches the requested voltage. The algorithm that implements this behavior is called load line compensation and it is integrated into all of the PIV-Q tests. There are 4 parameters that control the behavior of the load line compensation, to permit flexibility to test the widest possible range of transistors.

## RF Transistors and Oscillation

Oscillation is a fairly common occurrence when pulse testing RF transistors, especially on devices made from compound semiconductor (III-V) materials. This is due to the fact that RF transistors have a high frequency cutoff or threshold ($F_C$ or $F_T$), which means they are inherently unstable, primarily due to feedback paths. These feedback paths allow undesirable signals to be amplified, causing oscillation or ringing. An analogy to this would be the familiar screeching or high pitched whine of feedback in a public address system.

These feedback paths may be intrinsic, or contained within the device or its on-wafer interconnect. Or they may be extrinsic, due to the instrument or associated cabling. Generally, it is not possible to

eliminate all of these feedback paths, as some stray capacitance or other effect permits feedback at a given test condition for certain frequency or frequencies. The preferred way to retard oscillation is to reduce the loop gain of the transistor. This is typically done by adding a resistance to the gate or drain signal path, or both. As shown in Figure 3, this is usually done with a series resistance in the gate path and/or a parallel (or shunt) resistance in the drain. These stabilization resistors reduce the loop gain of the transistor and are usually available in a range of values. Because the oscillation starts at the DUT, it is important to insert these stabilization resistors as close as possible to the DUT. When using one or both of these types of stabilization resistors, the test software should subtract out the effect of the resistors, leaving just the DUT behavior. For example, $R_P$ is a parallel, or shunt, leakage path for $V_D$. The software should take this into account by subtracting $I_{RP} = V_D/R_P$ before reporting the DUT $I_D$.

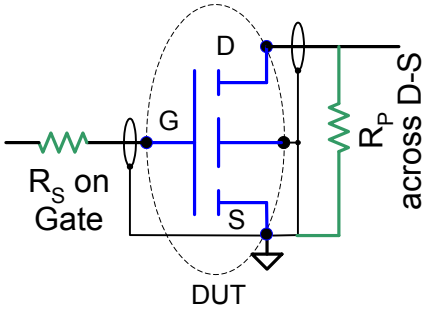


***Figure 3.*** *DUT with both types of stabilization resistors: series ($R_S$) on gate and parallel ($R_P$) across the drain-source.*

The overall approach of using the stabilization resistors is to minimize the disturbance to the overall test system capabilities which maximizes the voltage and current envelope available for the DUT and provides the best possible measurement results.

When first adding a stability resistor to address oscillation, it is preferable to start with a small $R_S$ on the gate. There are two reasons for this: 1) $R_S$ consumes less pulse power than $R_P$ on the drain, leaving more pulse power available for the DUT; 2) A smaller $R_S$ means a smaller voltage drop across $R_S$, resulting in more voltage available for the DUT Gate and minimizing the effect of the error in $V_G$ introduced by $R_S$. For the drain, there is a similar logic, but the starting value for $R_P$ across the drain-source should be large, to minimize the amount of current flowing through $R_P$ and minimize the error in the reported $I_D$.

Note that there are two main parameters that should be minimized: 1) Amount of pulse power dissipated in the stabilization resistor, which is not available for the DUT; 2) Minimizing the amount of error in the signals applied to the DUT. These two effects are the trade-off for using the stability resistors. Of course, if the system will only provide acceptable DUT results with a large $R_S$ on the DUT gate and a small $R_P$ on the drain, then that is the trade-off for obtaining useful results.

# PIV-Q Connections

The PIV-Q package uses two SMA cables to connect from the 4200 chassis to the DUT. These cables carry either the DC signals or pulse IV signals. For testing RF transistors use RF G-S-G probes and test structures.

On-wafer non-RF transistors, such as LDMOS transistors used for switching power supplies, use a DC pad layout, not a G-S-G layout. Therefore adapters are necessary to convert the SMA connections for the gate and drain to the appropriate type for low impedance DC connections. Note that probe tips with integrated triax cabling are not appropriate for pulse IV testing, as they do not easily permit the interconnections between the coax shields to reduce the loop area, which results in large inductance that prevents pulse transmission.

The most common DC probe connector type compatible with low impedance connection is the SSMC, which is available for most DC probe manipulators used on analytical probers:

- Cascade DCM-2xx DC probe manipulators
- Suss Microtec probe manipulators
- Signatone SCA-50 coaxial probes
- Any probe interconnect with SSMC connectors near the probe tip
    - American Probe & Technologies Series 73APT Low Current Coaxial Probes

In addition to SSMC connectors on probe holders or adapters, there are other connector types. For the 3 most common, SSMC, SMA and SMB, there are three types of adapters cables, which are not included with the PIV-Q package and must be ordered separately. Note that regardless of the connector type, the connections for the Y adapter cables must be located on the probe needle holder, as shown in Figure 8b, to minimize impedance mismatches and inductance.

For Pulse IV testing with DC probes, use one of the following adapter cable types listed in Table 1, noting that a quantity of 2 are required for a PIV-Q system.

***Table 1.*** *Adapter cables for use on analytical probers with DC probes*

| Keithley Model Number | Description | Quantity required for PIV-Q |
|---|---|---|
| 4200-PRB-C | SMA to dual SSMC (Figure 4a) | 2 |
| 4200-PRB-C-SMA | SMA to dual SMA (Figure 4b) | 2 |
| 4200-PRB-C-SMB | SMA to dual SMB (Figure 4c) | 2 |

***Figure 4a.*** *4200-PRB-C SMA to dual SSMC Y adapter cable for pulse IV with DC probes.*

***Figure 4b.*** *4200-PRB-C-SMA SMA to dual SMA Y adapter cable for pulse IV with DC probes.*

***Figure 4c.*** *4200-PRB-C-SMB SMA to dual SMB Y adapter cable for pulse IV with DC probes.*

Whether using G-S-G or DC interconnects, the cabling at the back of the 4200-SCS chassis is the same. A block diagram is shown in Figure 5 and a detailed connections diagram in Figure 6. When using DC layout DUTs, the addition of one type of adapter, shown in Figure 4a-c and Table 1, is required.

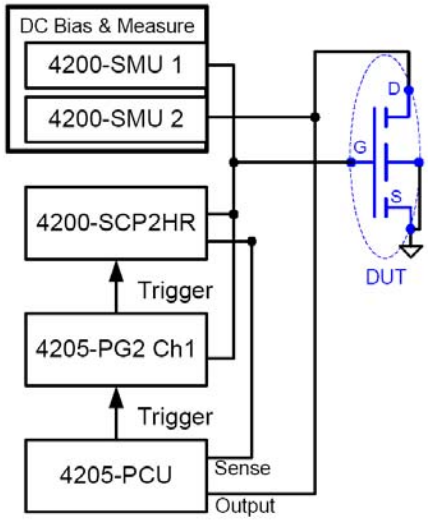


***Figure 5.*** *Block diagram of 4200-PIV-Q*

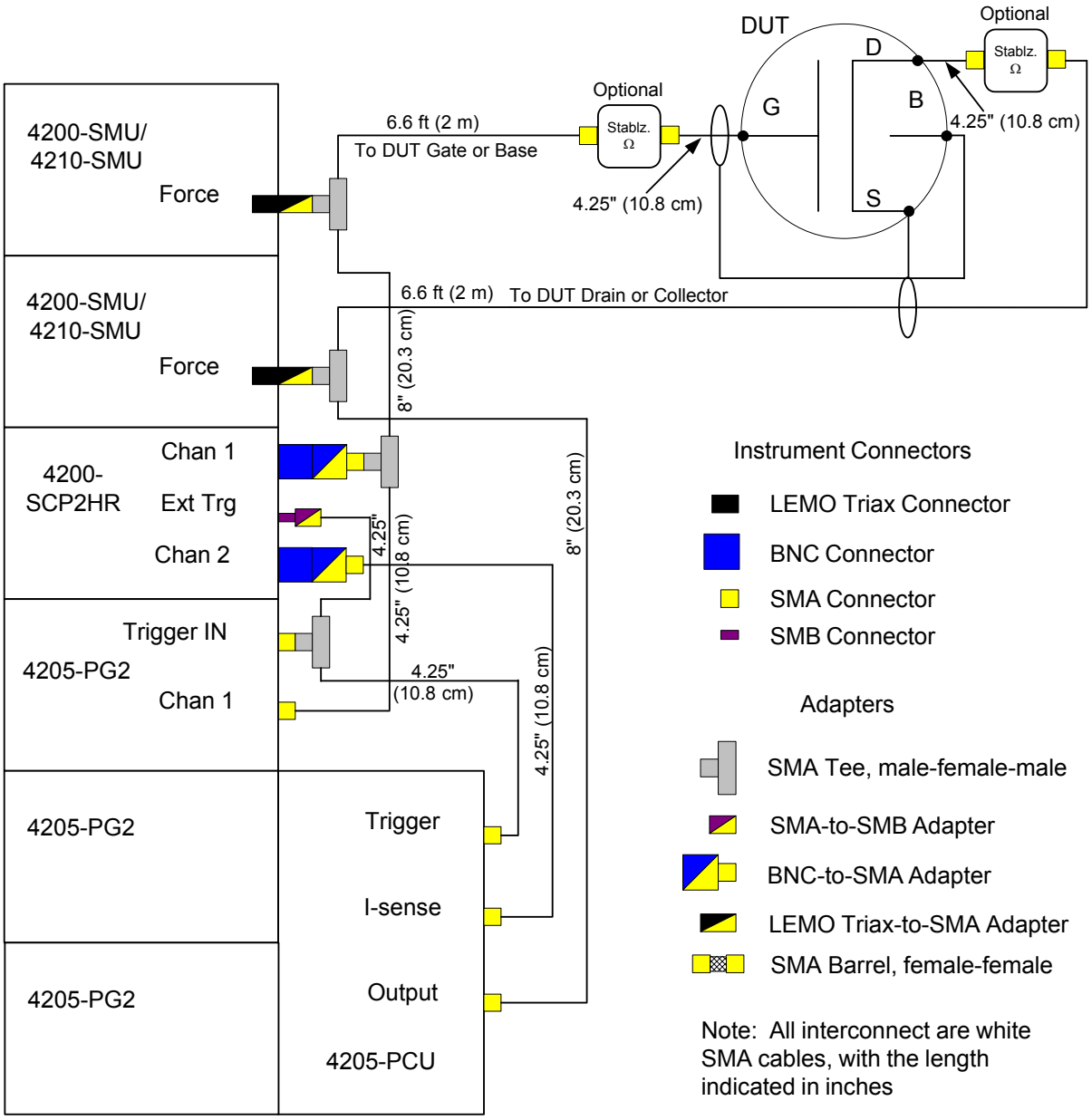


***Figure 6.*** *Connection Diagram for 4200-PIV-Q*

***Table 2.*** *Interconnect Parts for PIV-Q*

| Qty | Description | Comment |
|---|---|---|
| 4 | 4.25 in (10.8) cm white SMA cables | Interconnect for triggering |
| 2 | 8 in (20.3 cm) white SMA cables | Interconnect between pulse and DC signals |
| 2 | 6.6 ft (2 m) white SMA cables | Pulse Source + DC source-measure interconnect between instrument and DUT |
| 4 | Female-Male-Female SMA Tees | Trigger, Pulse + DC interconnect |
| 2 | LEMO triax-to-SMA Female | Adapt SMU Force output to SMA for signal interconnect |
| 2 | SMA Female to BNC Male | Convert SCP2 inputs to SMA |
| 1 | SMA Female to SMB plug | Convert SCP2 trigger input to SMA |
| 7 | SMA Male to MMBX | Convert SMA to MMBX for 4205-PCU |
| | | |
| | **4200-Q-STBL-KIT Stabilization Kit (optional)** | |
| 2 | 4.25 in (10.8 cm) white SMA cable, straight | Straight SMA to SMA connectors |
| 2 | 4.25 in (10.8 cm) white SMA cable, straight-90° | Straight SMA connector to 90° SMA connector |
| 2 | 6 in (10.8 cm) white SMA cable | |
| 2 | SMA Barrel Adapter, female-to-female | Used in place of stabilization resistor boxes |
| 2 | Stabilization Resistor boxes, empty | Allows customer to populate with custom resistor values. |
| | **Stabilization Resistor Values** | |
| | Series $R_S$ (Figure 12) | Parallel (shunt) $R_P$ (Figure 12) |
| 1 | 100 Ω | 10 Ω |
| 1 | 200 Ω | 50 Ω |
| 1 | 500 Ω | 100 Ω |
| 1 | 1 kΩ | 200 Ω |
| 1 | 2 kΩ | 500 Ω |

***Table 3.*** *Tools supplied with the 4200-SCS or PIV-Q package*

| Qty | Description |
|---|---|
| 1 | #1 Philips screwdriver |
| 1 | Torque wrench, 8 in/lb, with 5/16 in head installed |
| 1 | 4205-PCU alignment tool |

**Perform the following steps to connect:**

NOTE Refer to Figure 6 (connection diagram) and Figure 7 (instrument connections photo) for the following procedure. Use the supplied torque wrench to tighten each connection as it is assembled. Whenever possible, torque adapter and cable assemblies before attaching to instruments, to reduce any non-axial stress on the bulkhead connectors on the scope or pulse cards.

1. Set up the 4200-SCS, referring to the 4200-SCS Quick Start Guide and 4200-SCS Reference Manual (Sections 2, 4).
2. (Optional but recommended): Remove the 4205-PCU. It is easier to attach the SMA tee to the Trigger In and SMA cable to Channel 1 of the right 4205-PG2 with the PCU removed. Use the screwdriver to loosen the screws and remove the PCU. Use the white plastic alignment tool to ensure that the MMBX connectors on the inside of the PCU are aligned perpendicular to the PCU circuit board. Set aside for later use.
3. Attach two 4.25 in (10.8 cm) cables to a SMA tee. Torque using wrench.
4. To one of the cables from above, connect the SMA to SMB adapter. Torque using wrench.
5. Connect SMA Tee from above to the Trigger IN of the 4205-PG2 in the lowest numbered slot. The Tee should be oriented nearly vertically, with the SMB adapter cable pointing down, as shown in Figure 5. Torque using wrench.

6. Connect the SMA cable from above, with the SMB adapter, to the Ext Trg on the SCP2. Use care whenever connecting or disconnecting the SMB cable. Ensure that the connector is aligned with the SMB connector and is perpendicular to the back panel.
7. Connect one 4.25 in (10.8 cm) cable and one 8 in (20.3 cm) cable to another SMA Tee. Torque using wrench.
8. Connect one SMA to BNC adapter to the Tee from above. Torque using wrench.
9. Connect the free end of the 4.25 in (10.8 cm) cable from above to Channel 1 of the 4205-PG2 in the lowest numbered slot. Torque using wrench.
10. Connect the SMA-BNC adapter from above to Channel 1 of the SCP2.
11. To the other end of the 8 in (20.3 cm) cable from above, attach a SMA Tee. Torque using wrench.
12. To the Tee from above, attach a LEMO-to-SMA adapter. Torque using wrench.
13. To the Tee from above, connect a 6.6 ft (2 m) SMA cable. Torque using wrench.
14. Install the Lemo adapter from above into SMU1.
15. Route 6.6 ft (2 m) cable to DUT gate. Do not connect to the DUT.
16. Optional: If using the 8101-PIV test fixture and DUT. Connect SMA cable from above to the AC+DC IN 1 (Gate) connection.
17. For RF DUT testing, connect SMA barrel to end of 6.6 ft (2 m) cable then connect 4.25 in (10.8 cm) cable, both included in the optional stabilization kit. If testing DUTs that will not require any stabilization resistors, this step can be skipped.
18. Connect 4.25 in (10.8 cm) cable, from stabilization kit, to SMA barrel and opposite end to DUT gate GSG probe.
19. If the PCU was removed, install PCU now, being careful to align the connectors as the PCU housing is pressed onto the two 4205-PG2 cards in the highest numbered slots. Use the screwdriver to tighten down the PCU screws. Start each screw before final tightening.
20. Using the last 4.25 in (10.8 cm) cable, connect a SMA to BNC adapter. Torque using wrench.
21. Connect SMA cable from above to the PCU Sense. Torque using wrench.
22. Connect BNC adapter from above to Channel 2 of the SCP2.
23. Using the last SMA Tee, connect the last 8 in (20.3 cm) SMA cable. Torque using wrench.
24. Connect a LEMO-to-SMA adapter to the Tee from above.
25. Connect a 6.6 ft (2 m) SMA cable to the Tee from above.
26. Connect the 8 in (20.3 cm) cable from above to the PCU Output. Torque using wrench.
27. Connect the LEMO adapter from above to a SMU. Use a high power 4210-SMU if available.
28. Route 6.6 ft (2 m) cable to DUT drain. Do not connect to the DUT.
29. Optional: If using the 8101-PIV test fixture and DUT. Connect SMA cable from above to the AC+DC IN 2 connection.
30. For RF DUT testing, connect SMA barrel to end of 6.6 ft (2 m) cable then connect 4.25 in (10.8 cm) cable, both included in the optional stabilization kit. If testing DUTs that will not require any stabilization resistors, this step can be skipped.
31. For RF DUT testing, connect unused end of the 4.25 in (10.8 cm) cable from the previous step the DUT drain GSG probe (Figure 8a). If connecting to DC probes, follow the instructions included with the appropriate Y adapter cables (Table 1) and Figure 8b.

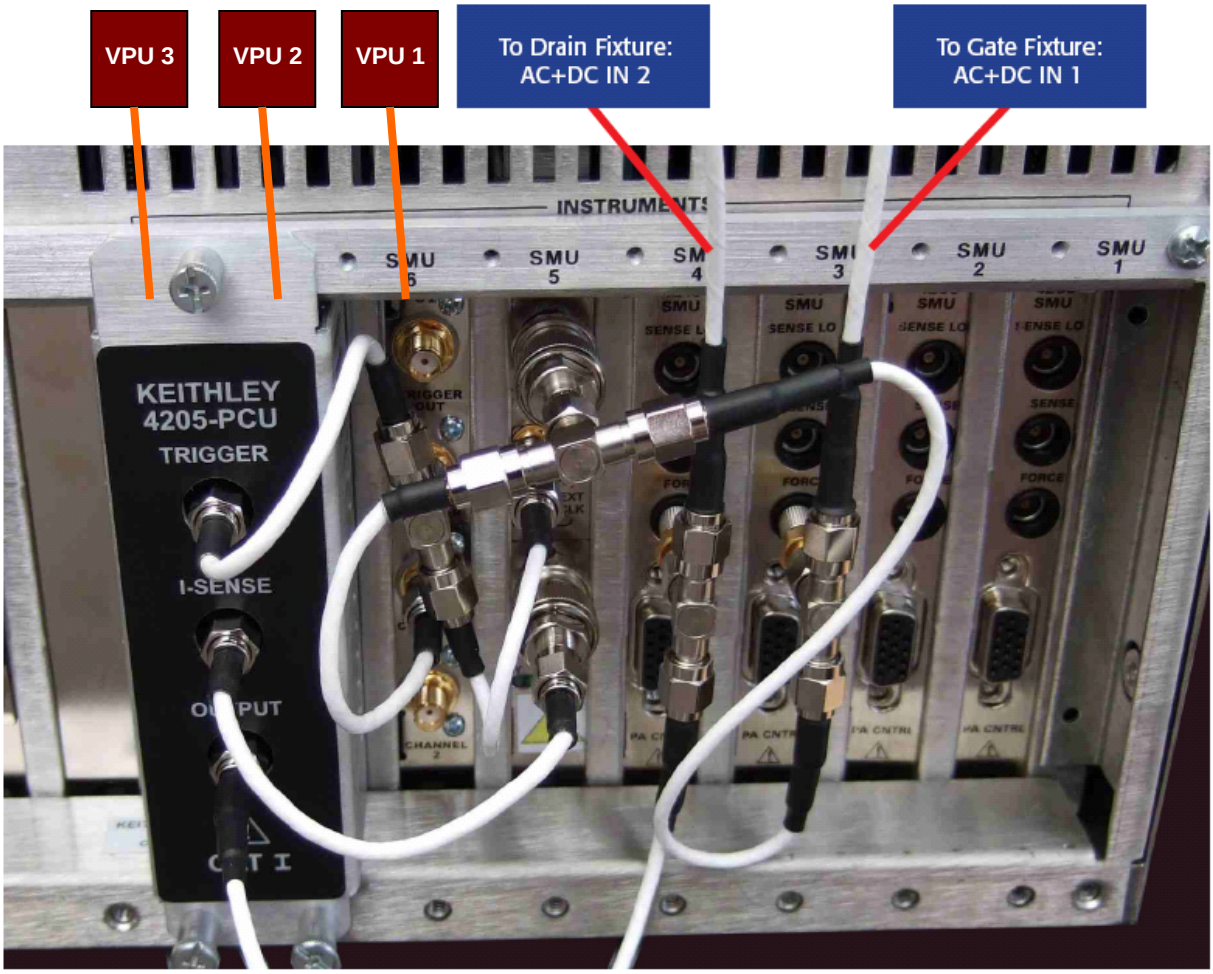


***Figure 7.*** *Photograph of PIV-Q connections*

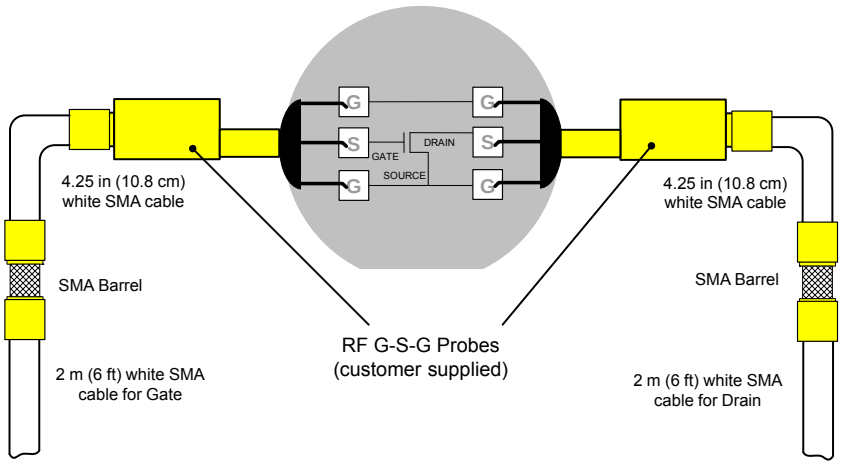


***Figure 8a.*** *G-S-G connection diagram for RF transistors. The SMA barrels are used during Cable Compensation, and then replaced with stabilization resistors if necessary.*

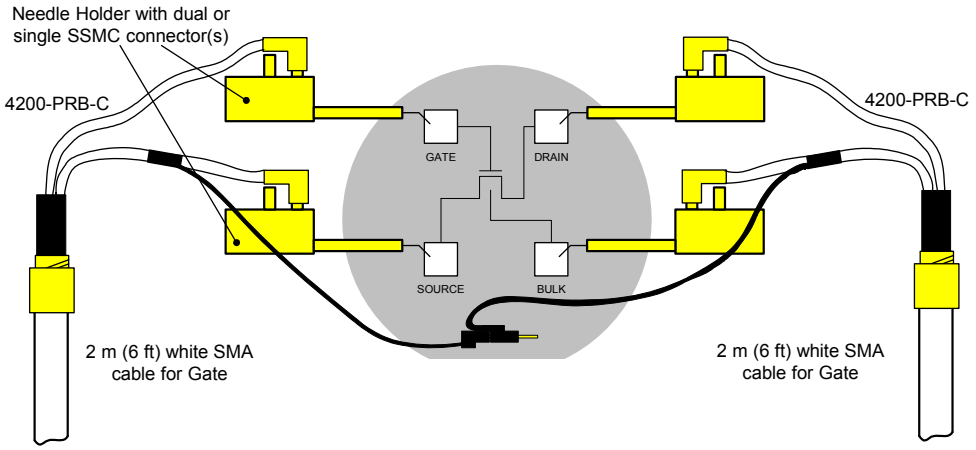


***Figure 8b.*** *Connection diagram for transistors with DC layout. This interconnect method is not appropriate for RF transistors, or for any test requiring high bandwidth signal transmission.*

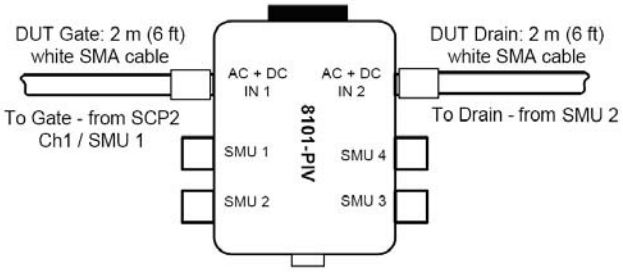


***Figure 9a.*** *Connection from PIV-Q cables to 8101-PIV test fixture.*

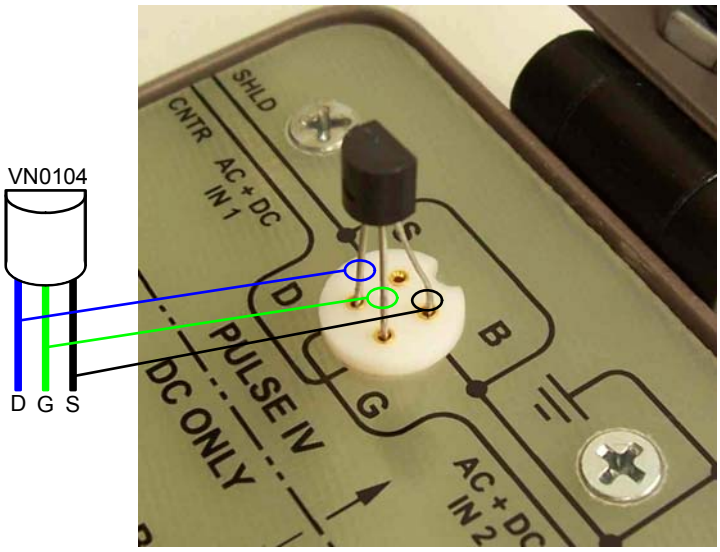


***Figure 9b.*** *Photograph of PIV-Q DUT (Supertex VN0104N3), with pinout, installed in 8101-PIV test fixture. As shown, the Source (S) pin must be bent appropriately to fit into the "B" socket. Note that S and B pin sockets are shorted together, as shown in Figure 9b and on the schematic of the 8101-PIV.*

**Stabilization Kit (4200-Q-STBL-KIT)**

The 4200-Q-STBL-KIT is an optional item that can be ordered with the 4200-PIV-Q, or added later. It consists of 10 parallel (shunt) and series resistor values to address system oscillation. Figure 10 shows the case for the kit, while figure 11 shows an example of one of the stabilization resistor boxes.

***Figure 10.*** *4200-Q-STBL-KIT case*


***Figure 11.*** *Photo of one of the stabilization resistors, showing the SMA connections on either side.*

***Table 4.*** *Contents of the 4200-Q-STBL-KIT*

| Qty | Item description |
|---|---|
| 1 | 100 Ω Series Stabilization Resistor |
| 1 | 200 Ω Series Stabilization Resistor |
| 1 | 500 Ω Series Stabilization Resistor |
| 1 | 1 kΩ Series Stabilization Resistor |
| 1 | 2 kΩ Series Stabilization Resistor |
| 1 | 10 Ω Parallel Stabilization Resistor |
| 1 | 50 Ω Parallel Stabilization Resistor |
| 1 | 100 Ω Parallel Stabilization Resistor |
| 1 | 200 Ω Parallel Stabilization Resistor |
| 1 | 500 Ω Parallel Stabilization Resistor |
| 2 | Blank Stabilization Resistor* |
| 2 | SMA Cable, 6 inch (15 cm) |
| 2 | SMA Cable, 4.25 inch (10.8 cm) |
| 2 | SMA Cable with one right angle connector, 4.25 inch (10.8 cm) |
| 2 | SMA Barrel, male-male |

* Two blank stabilization resistor boxes are provided to simplify use of customer-provided resistance values.

Although the test software compensates for the stabilization resistors, the addition of these resistors does affect the system performance. When adding a series resistance to the gate, the available voltage output to the gate is somewhat reduced, as there is an additional voltage drop across the series resistance, $R_S$, reducing the voltage available at the device gate. Also, the accuracy of the voltage applied to the gate is

decreased, which may cause shifts in $V_D$-$I_D$ curves. Additionally, on the drain, adding a parallel or shunt resistor reduces the amount of current available for the DUT. To minimize the affect of the stabilization resistors on the available test envelope, start with smaller series resistance values on the gate, or larger parallel (shunt) resistors on the drain. The two types of stabilization resistors are shown schematically in Figure 12. See Figure 3 for a diagram showing both the stabilization resistors and the DUT.

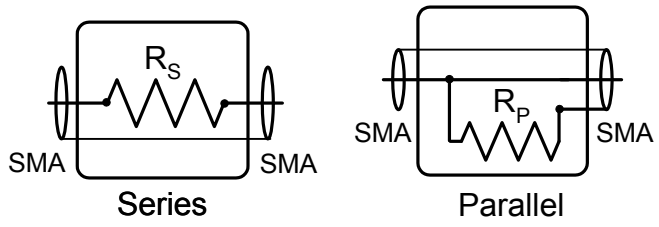


***Figure 12.*** *Two types of stabilization resistors boxes.*

To provide optimal retardation of oscillation, these stabilization, or ballast, resistors should be located as close as possible to the DUT. In practice, packaging, connecting and power-handling concerns of the stabilization resistors deviate from the ideal. These deviations may allow for some oscillation or instability for certain device types or test conditions.

Because of the wide range of possible interactions and potential parameters, the process of choosing the stabilization type (series or parallel) or the particular resistance value is iterative.

There are two methods used to detect oscillation or the onset of oscillation. Experienced users are able to notice the perturbations in the $V_D$-$I_D$ curves. Another method is to view the pulse waveforms by using an included test module that displays the pulse waveform, similar to an oscilloscope view. These two methods are complementary and will be covered further below.

The test projects included with the 4200-PIV-Q package include parameters to specify the stabilization resistor value and type, so the software can provide corrected results.

**Maximum Voltage and Current for the Drain and Gate**

The 4200-PIV-Q package uses a fixed output impedance voltage pulse source, similar to many pulsers available on the market. This means that the voltage and current available at the DUT is a function of the DUT resistance. Pulse sources do not typically have any sense feedback and therefore output a signal based on a user-supplied, or default, DUT impedance. The 4200-PIV-Q package assumes that the DUT impedance is 50 Ω for both the gate and drain when sourcing a voltage, but the Load Line Compensation algorithm measures the actual gate and drain voltage and modifies the pulse level to reach the requested voltages.

As shown in Figure 13, the pulse source for the drain has 55 ohm output impedance. As current flows, voltage drops across both the 50 Ω and 5 Ω resistors. There are two ranges for the pulse source on the drain: 10V and 40V.

Figures 14 and 15 show the maximum drain-source voltage and current. Note that Figure 15 zooms in on the left-hand portion of Figure 14, illustrating the maximum I and V for drain-source resistances < 100 Ω. Table 5 shows available $I_{DMAX}$ and $V_{DMAX}$, based on various $R_{DS}$ values. Note that the $R_{DS}$ values are necessary to calculate the maximum $V_D$ and $I_D$ available for a given impedance, but are not required when performing PIV-Q tests with the Load Line Compensation enabled.

***Table 5.*** *Maximum DUT Drain current and voltage for PIV-Q*

| Max Drain Source using 40V Range (Vs = 80V), typical | | | Max Drain Source using 10V Range (Vs = 22V), typical | |
|---|---|---|---|---|
| Maximum* $V_D$ (V) | Maximum* $I_D$ (A) | $R_{DS}$ (Ω) | Maximum* $V_D$ (V) | Maximum* $I_D$ (A) |
| 6.65 | 1.33 | 5 | 1.83 | 0.366 |
| 12.3 | 1.23 | 10 | 3.38 | .338 |
| 25 | 1.0 | 25 | 6.87 | .275 |
| 38 | 0.76 | 50 | 10.47 | .210 |
| 50 | 0.54 | 92 | 13.78 | .150 |
| 51.6 | 0.51 | 100 | 14.19 | .140 |
| 65 | 0.26 | 250 | 18.03 | 0.072 |
| 75.8 | 0.075 | 1k | 20.00 | 0.019 |

* Approximate maximum, does not account for interconnect losses.

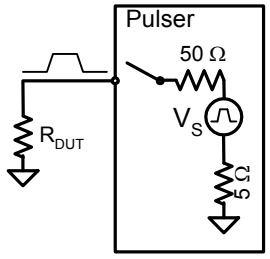


***Figure 13.*** *Simplified Block diagram of the PIV-Q pulse source for the DUT drain.*

NOTE: The maximum voltage is reached when the DUT drain-source impedance reaches a large value (≥10 k Ω). The corresponding current through the DUT is low. This behavior, high voltage with low current, is the result of the pulser circuitry. Looking at Figure 13, there is just a pulse source, $V_S$, with a 55 Ω of impedance. The specification for the maximum voltage on the drain for 4200-PIV-Q is 38 V into 50 Ω. The maximum $V_S$ of the pulser is 80V for the 40V range. Since Ohm's Law applies for a pulse source, here are examples that supply typical values:

Example 1: $R_{DUT\ D\text{-}S}$ = 50 Ω

V=I * R
$I_{MAX\ DRAIN} = V_{MAX} / R_{TOTAL} = V_{MAX} / (R_{PULSER} + R_{DUT})$
$I_{MAX\ DRAIN}$ = 80 V / (55 Ω + 50 Ω) = 80 / 105 = 761.9 mA
And $V_{MAX\ DUT\ DRAIN} = R_{DUT\ D\text{-}S} * I_{MAX\ DRAIN}$ = 50 Ω * 760 mA = 38 V

Ohm's Law can verify the maximum specifications of the drain pulse parameters. See the vertical dotted line, at 50 Ω, in Figure 15.

Of course, the drain-source impedance is rarely exactly 50 Ω.

Example 2: $R_{DUT\ D\text{-}S}$ = 10 Ω

V=I * R
$I_{MAX\ DRAIN} = V_{MAX} / R_{TOTAL} = V_{MAX} / (R_{PULSER} + R_{DUT})$
$I_{MAX\ DRAIN}$ = 80 V / (55 Ω + 10 Ω) = 80 / 65 = 1.23 A
And $V_{MAX\ DUT\ DRAIN} = R_{DUT\ D\text{-}S} * I_{MAX\ DRAIN}$ = 10 Ω * 1.23 A = 12.3 V

These values correspond to the vertical dotted line, at 10 Ω, in Figure 12.

Example 3: $R_{DUT\ D\text{-}S}$ = 100 Ω

V=I * R
$I_{MAX\ DRAIN} = V_{MAX} / R_{TOTAL} = V_{MAX} / (R_{PULSER} + R_{DUT})$
$I_{MAX\ DRAIN}$ = 80 V / (55 Ω + 100 Ω) = 80 / 155 = 516 mA
And $V_{MAX\ DUT\ DRAIN} = R_{DUT\ D\text{-}S} * I_{MAX\ DRAIN}$ = 100 Ω * 516 mA = 51.6 V

NOTE: All of these examples illustrate the effect of $R_{DUT}$ on the available current and voltage, but actual values are effected by the impedance of the interconnect, which will reduce the voltage available at the DUT.

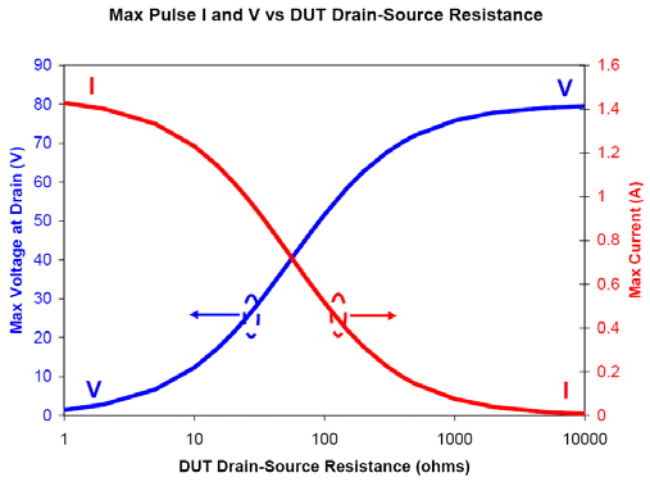


***Figure 14.*** *Maximum drain-source voltage and current, log x scale.*

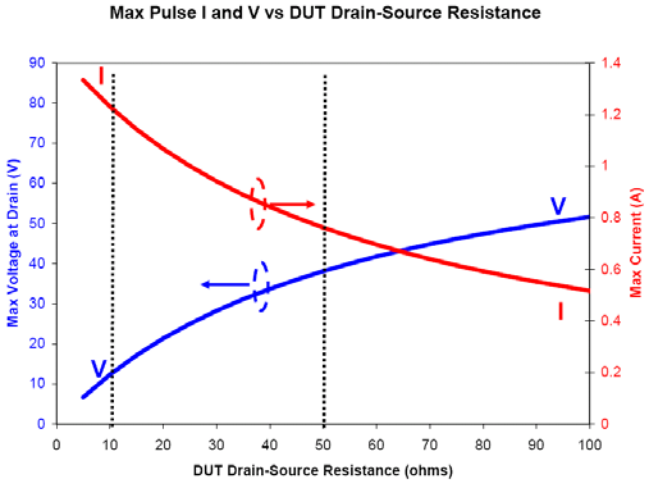


***Figure 15.*** *Maximum drain-source voltage and current, linear x scale.*

Figures 14 and 15 show that the maximum drain current occurs when the drain-source resistance is low and the highest voltage occurs when the drain-source impedance is high. This matches the expected performance, as the output characteristics are determined by Ohm's law (V = I * R). As shown in Figure 13, the resistance seen by the pulse source is the 55 ohms of the pulser plus the drain-source resistance.

Similar logic applies for the Gate, but the maximum Vs is as shown in Table 6, and the output impedance is 50 Ω.

***Table 6.*** *Maximum DUT Gate current and voltage for PIV-Q*

| Max Gate Source using 20V Range (Vs = 40V), typical | | | Max Gate Source using 5V Range (Vs = 11V), typical | |
|---|---|---|---|---|
| Maximum* $V_G$ (V) | Maximum* $I_G$ (A) | $R_G$ (Ω) | Maximum* $V_G$ (V) | Maximum* $I_G$ (A) |
| 3.6 | 0.769 | 5 | 1 | 0.200 |
| 6.67 | 0.667 | 10 | 1.83 | 0.183 |
| 13.3 | 0.533 | 25 | 3.67 | 0.147 |
| 20 | 0.400 | 50 | 5.5 | 0.110 |
| | | 92 | 7.13 | 0.077 |
| | | 100 | 7.33 | 0.073 |
| | | 250 | 9.17 | 0.037 |
| | | 1k | 10.4 | 0.010 |

* Approximate maximum, does not account for interconnect losses.

## Load Line Compensation

The effect of resistance in the system and interconnect causes voltage drops when current flows. When a resistance is used to measure a current (also called a shunt ammeter), there is a voltage drop across the sense resistor when current flows through the sense resistor. In both cases, this voltage drop is called the load line effect. So, the load line effect can be summarized that the voltage at the DUT is less than desired, due to the voltage drop across the sense resistor, and other impedances in the system. For very small currents, or small sense resistors (< 1 ohm), this load line effect may be too small to worry about. But, with larger sense resistors, or other large resistances in the interconnect, or much larger currents, the load line effect can easily be 5-20V, meaning that the voltage at the DUT could be lower than the source voltage by this same 5-20V.

Of course, it is useful to be able to compensate for this voltage drop caused by the load line effect. Software algorithms can use the measured current, along with the system resistances, to compensate for the load line effect. The algorithm calculates the load line effect voltage drop, then increases the source voltage, iterating until the desired voltage is reached. The software included with the 4200-PIV-Q package allows for independent On/Off control of the load line compensation for the gate and drain, as well as controlling the number of attempts the algorithm uses to reach the desired voltage.

Since the pulsers used in the 4200-PIV-Q package have a fixed output impedance, this is the dominating resistance that causes voltage drops when current flows. Of course, most current flows through the drain, so that is where the load line effect is the greatest. Figure 16 shows a single $V_D$-$I_D$ curve with the load line compensation on and off and Table 7 summarizes the differences of enabling or disabling Load Line Compensation.

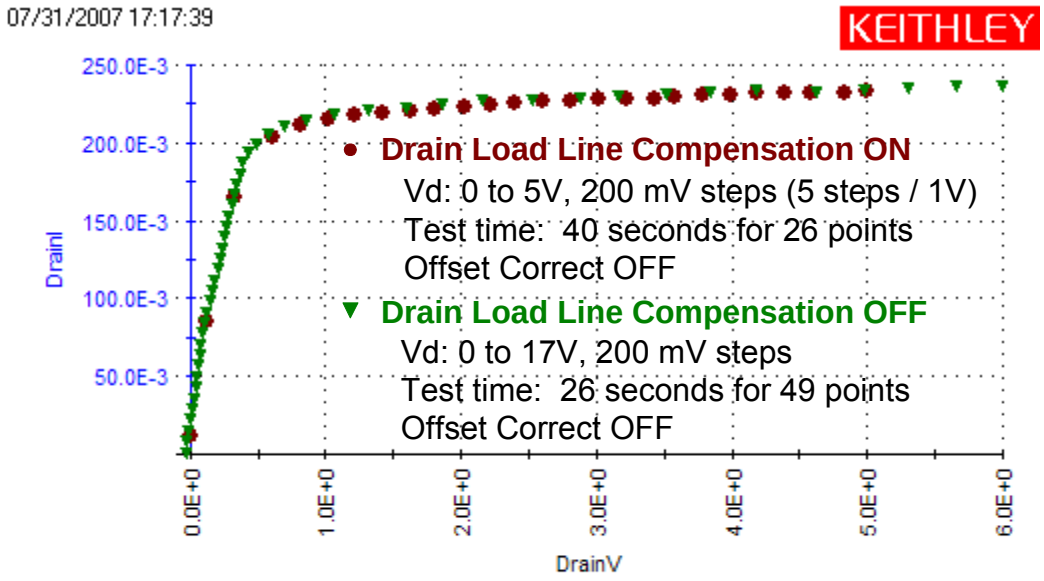


***Figure 16.*** *Effect of Load Line Compensation on a $V_D$-$I_D$ curve. Note the even spacing for the red circles. The green triangles, load line correction disabled, have an uneven spacing, with many points close together at the start of the curve, then less and less as $V_D$ increases.*

***Table 7.*** *Comparison: Load Line Compensation On and Off (Figure 14) on Demo DUT.*

| Attribute | Load Line Compensation | |
|---|---|---|
| | ● ON (Red circles) | ▼ OFF (Green triangles) |
| $V_D$ spacing | 200 mV, as desired | Varies (10 mV to 350 mV), due to load line effect |
| Number of points | 26, as desired | 49, varies from curve to curve |
| Test Time | 40 seconds | 26 seconds |
| Benefit | Accurate $V_D$ spacing | Shorter test time and eliminates any instability (“zig-zag”) in the curve due to improper Load Line Compensation |
| Drawback | Possible mis-spacings during linear portion of $V_D$-$I_D$ curve. “zigzag” results on high gain devices, especially during DUT transition from linear to saturation | $V_D$ spacing varies across $V_D$-$I_D$ curve |

## 4200-PIV-Q Test Projects

There are two projects included with the PIV-Q package:

- QPulseIV-Complete
- QPulseIV-Demo

QPulseIV-Complete is located in the path C:\S4200\kiuser\Projects_Pulse.

QPulseIV-Demo is located in C:\S4200\kiuser\Projects_Demo.

These two projects contain mostly the same tests, detailed below, but QPulseIV-Demo has been optimized for demonstrating the PIV-Q package on the PIV-Q demo DUT and 8101-PIV test fixture (Figures 9a-b).

There is one difference in the tests, QPulseIV-Complete has a Measure_Stability_Resistor test as part of the Initialization Steps, which is used to measure the series or parallel resistance of stability resistors used to address system oscillation on compound semiconductor RF transistors.

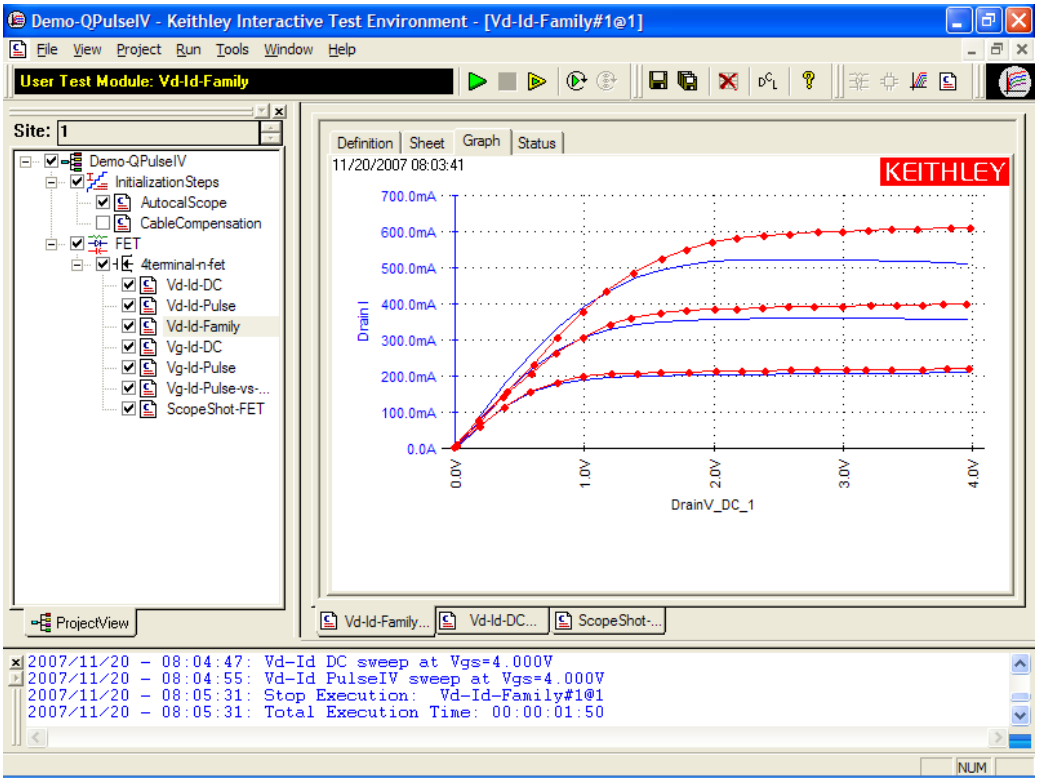


***Figure 17.*** *Screenshot of the Demo-QPulseIV project, showing a $V_D$-$I_D$ family of curves graph with the DC curves in blue (solid line) and the pulse IV curves in red (line with data point dots).*

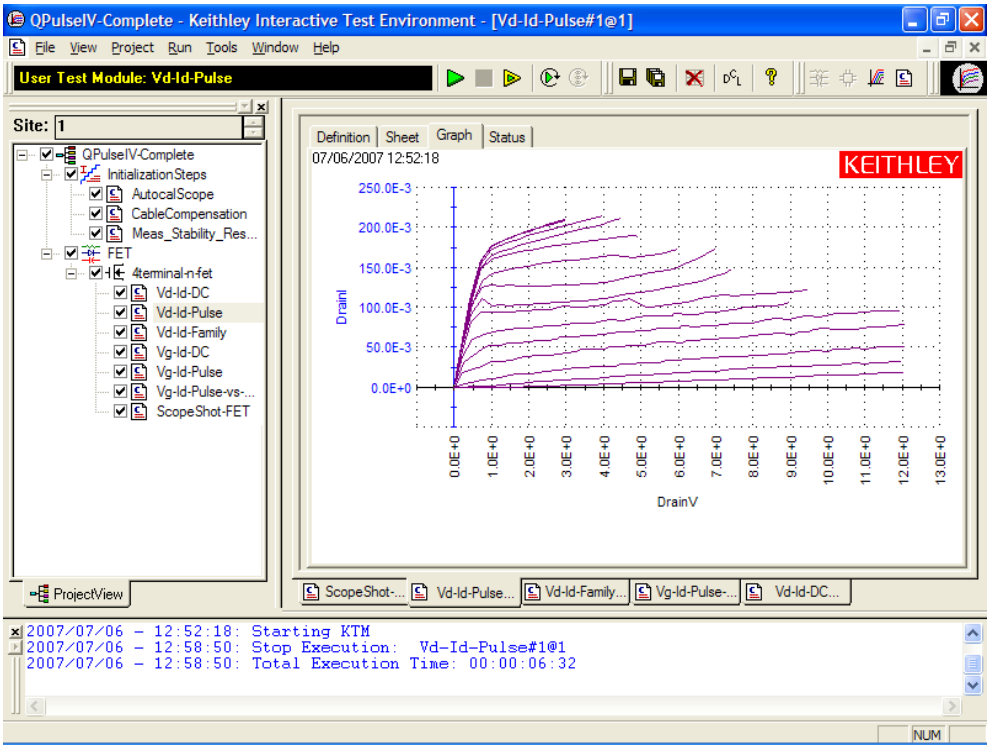


***Figure 18.*** *Screenshot of the QPulseIV-Complete project, showing a $V_D$-$I_D$ family of curves graph.*

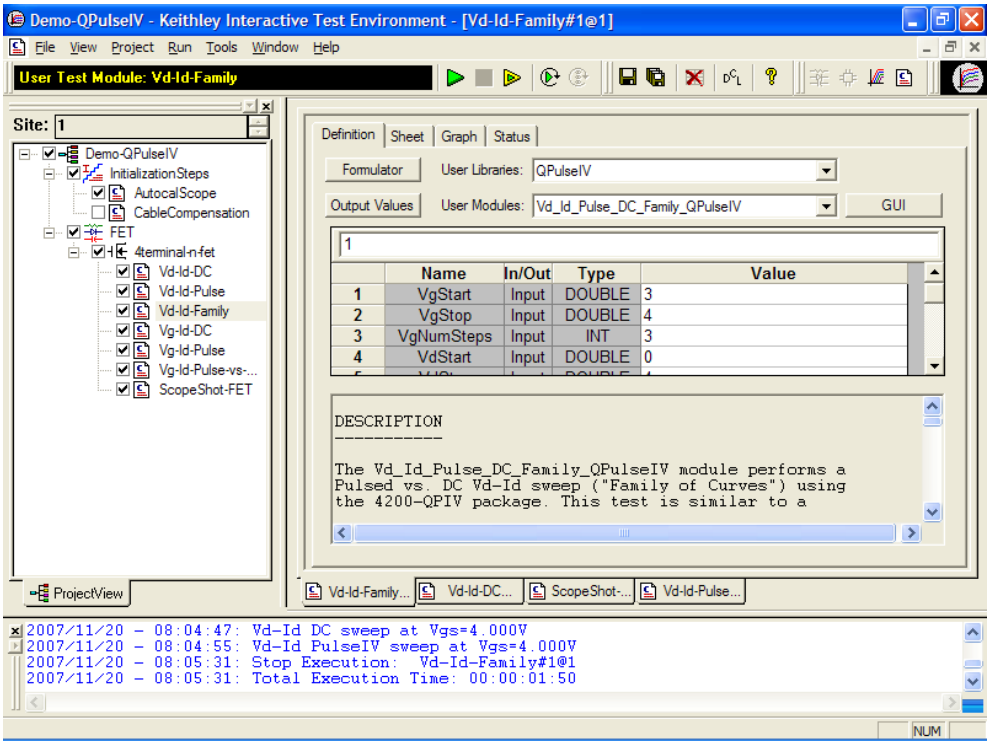


***Figure 19.*** *Screenshot of Demo-QPulseIV Vd-Id-Family test definition. Note the Definition tab on the right side of the window, containing the parameter list (VgStart, VgStop, …) and the help section with the "Description" title.*

## Initialization Tests

**AutocalScope –** Runs the self calibration and offset measurement routine for the 4200-SCP2HR scope card. This routine should be run before every PulseIV cal and periodically to capture any drift in the scope. It requires all connections be removed from the scope and takes about 2-3 minutes.

**CableCompensation -** This is the Pulse-IV cable compensation routine that should be used during initial setup and whenever interconnects are changed. Before starting this routine, ensure that all stability resistors are removed from the system interconnect. This routine takes about 15-20 minutes and consists of 3 parts, which requires changing the connections twice, from an open, to a through, then back to an open. This routine is similar to an open/short calibration used for capacitance measurements, but the through connection does not consist of shorting the center (signal) pin to the shield. This routine should be performed during initial setup, after running AutocalScope. It should also be run after any changes in the interconnect.

**Measure_Stability_Resistance –** This test will measure either a series or parallel (shunt) stability resistor. The benefit of this test is to verify the resistance value, which can then be entered into one of the PIV-Q tests when the use of stability resistor(s) is (are) required. The use of this routine requires disconnecting the PIV-Q SMA cables from the probe manipulators and connecting to each stability resistor box to be measured, one at a time.

Because of the finicky nature of testing RF transistors, both PIV-Q projects have many parameters to allow for testing across a wide variety of settings, and includes the ability to trade off for measurement accuracy and test time.

## Explanation of QPulseIV-Complete Test Parameters

The parameter list below is a superset of all of the tests included with PIV-Q. Note that parameters used for the Initialization steps are covered separately. These explanations are also available within each test of the project, located on the lower portion of the Description tab for each test (Figure 19).

| | |
|---|---|
| VgStart | (double) The starting step value for Vg. For DC only sweeps, VgStart must be between -200V to +200V dependent on the type of SMU and the current requirements of the DUT. For pulse and pulse & DC Sweeps, VgStart must be between -5V to +5V or -20V to +20V depending on the specified source range for the PG2. |
| VgStop | (double) The final step value for Vg. For DC only sweeps, VgStop must be between -200V to +200V dependent on the type of SMU and the current requirements of the DUT. For pulse and pulse & DC Sweeps, VgStop must be between -5V to +5V or -20V to +20V depending on the specified source range for the PG2. |
| VgNumSteps | (double) The number of steps for Vg (Max = 13). |
| VdStart | (double) The starting sweep value for Vd. For DC only sweeps, VdStart must be between -200V to +200V dependent on the type of SMU and the current requirements of the DUT. For pulse and pulse & DC Sweeps,VdStart must be between -10V to +10V or -40V to +40V depending on the specified source range for the 4205-PCU. |
| VdStop | (double) The final sweep value for Vd. For DC only sweeps, VdStop must be between -200V to +200V dependent on the type of SMU and the current requirements of the DUT. For pulse and pulse & DC Sweeps, VdStop must |

| | |
|---|---|
| | be between -10V to +10V or -40V to +40V depending on the specified source range for the 4205-PCU. |
| VdStep | (double) The number of steps for the Vd sweep. (Max = 10,000). Note that the number of steps must ≤ data array sizes (see below). |
| VgQPoint | (double) The base value, or bias point, of the pulsed gate source. VgQPoint is range dependent and must be between -5V to +5V or -20V to +20V. |
| VdQPoint | (double) The base value, or bias point, of the pulsed drain sweep. VdQPoint is range dependent and must be between -10V to +10V or -40V to +40V. |
| PulseWidth | (double) The Vgs and Vds pulse width (PW). The Pulse Width range: 500ns to 999.999 ms in 10ns resolution steps. |
| PulsePeriod | (double) The pulse period for Vgs and Vds. Minimum period is (FallTime/2) + (RiseTime/2) + PulseWidth + 10ns. Maximum period is 1s. |
| RiseTime | (double) The transition time from the Qpoint to the pulse value for both Vgs and Vds. The transition time is source range dependent. For the 5V range (10V for 4205-PCU) the minimum transition time is 10ns (recommended minimum is 50ns) and for the 20V range (40V for the 4205-PCU) the minimum transition time is 100ns. Using the default rise time of 150 ns provides the best results. The maximum transition time is dependent on the pulse width, period, and rise/fall time. |
| FallTime | (double) The transition time from the pulse to the Qpoint value for both Vgs and Vds. The transition time is source range dependent. For the 5V range (10V for 4205-PCU) the minimum transition time is 10ns (recommended minimum is 50ns) and for the 20V range (40V for the 4205-PCU) the minimum transition time is 100ns. Using the default rise time of 150 ns provides the best results. The maximum transition time is dependent on the pulse width, period, and rise/fall time. |
| PulseAverage | (int) The number of pulses to average to provide a single reading. A PulseAverage = 0 means the 4200 will use Adaptive Filtering, which is the use of variable averaging across the different scope ranges in order to provide maximum current measure resolution. The minimum recommended PulseAverage = 2. |
| GateVPURange | (double) The source range for gate side PG2. Valid ranges are 5V (High Speed) and 20V (High Voltage). |
| DrainVPURange | (double) The source range for the drain side 4205-PCU. Valid ranges are 10V (High Speed) and 40V (High Voltage). |
| GateSMURange | (int) The current measurement range to be used for the SMU on the DUT Gate terminal. Values correspond to the table below. Note that Limited Auto means that the value given is the minimum measurement range used, with automatic ranging for larger currents.<br>1 Full Auto<br>2 Limited Auto 10pA<br>3 Limited Auto 100pA<br>4 Limited Auto 1nA<br>5 Limited Auto 10nA<br>6 Limited Auto 100nA |

7 Limited Auto 1uA
8 Limited Auto 10uA
9 Limited Auto 100uA
10 Limited Auto 1mA
11 Limited Auto 10mA
12 Limited Auto 100mA

DrainSMURange — (int) The current measurement range to be used for the SMU on the DUT Drain terminal. Values correspond to the table below. Note that Limited Auto means that the value given is the minimum measurement range used, with automatic ranging for larger currents.

1 Full Auto
2 Limited Auto 10pA
3 Limited Auto 100pA
4 Limited Auto 1nA
5 Limited Auto 10nA
6 Limited Auto 100nA
7 Limited Auto 1uA
8 Limited Auto 10uA
9 Limited Auto 100uA
10 Limited Auto 1mA
11 Limited Auto 10mA
12 Limited Auto 100mA

GateScpRange — (double) The voltage measure range for the scope channel measuring the Gate. Use 0 for scope autoranging, or specify a voltage value for a fixed range. Note that the range is a full range value (for example, 2.5 is -1.25 V to +1.25 V).
Valid voltage ranges are 0.5, 1.25, 2.5, 5, 10, 25, 50.

DrainScpRange — (double) The voltage measure range for the scope channel measuring the Drain voltage across the 5 Ω sense resistor. Use 0 for scope autoranging, or specify a voltage value for a fixed range. Note that the range is a full range value (for example, 2.5 is -1.25 V to +1.25 V).
Valid voltage ranges are 0.5, 1.25, 2.5, 5, 10, 25, 50.

QPointLoadLine — (int) This parameter controls load line compensation for both the Gate and Drain while sourcing the QPoint values. When load line correction is turned off (set = 0), the specified voltages (VgQPoint, VdQPoint) will be sourced. Generally this parameter is set to 1 (Load Line Compensation enabled).
(1 = Use Load Line, 0 = No Load Line)

GateLoadLine — (int) Determines whether to use load line correction to compensate for the voltage drop caused by current flowing through the DUT Gate and gate-side system impedance. When load line correction is on (1), the test will start by assuming a high impedance value for the device and will approach the correct bias and pulse values over a series of pulses, which ensures that the sourced pulses match the requested values. When load line correction is turned off, the specified voltages will be sourced.
(1 = Use Load Line, 0 = No Load Line).

DrainLoadLine — (int) Determines whether to use load line correction to compensate for the voltage drop caused by the DUT impedance on the Drain and drain-side system impedance. When load line correction is on (1), the test will start by assuming a high impedance value for the device and will approach the correct bias and pulse values over a series of pulses, which ensures that the sourced

| | |
|---|---|
| | pulses match the requested values. When load line correction is turned off, the specified voltages will be sourced.<br>(1 = Use Load Line, 0 = No Load Line). |
| LoadLineIterations | (int) Determines the number of iterations of load line compensation to use. A higher number will permit better matching between the requested voltages and sourced voltages, but at the expense of longer test time. This value may need to be increased for high gain devices or any situation where voltage values for first point of the sweep are significantly different from the Q-point voltage values. |
| OffsetCorrect | (int) Determines if scope offset correction should be used during the test. Offset Correct will provide better accuracy by correcting for various scope and system offsets. There are three different modes, with OffsetCorrect = 1 recommended.<br>0 - No measurement correction performed; only recommended for system troubleshooting by a knowledgeable operator or engineer.<br><br>1 - System correction applied to measurements. The correction factors applied were measured during CableCompensation.<br><br>2 - Same as above, but the scope offset measurements taken at the start of the test are used in place of the scope offset measurements taken during CableCompensation. This approach may provide improved measurement results, but the pre-test offset measurement adds additional time to the test (30-45 s for PulsePeriod < 200 us and PulseAverage < 100. Longer PulseWidths or PulsePeriods or higher values for PulseAverage will increase the OffsetCorrect measurement time). |
| GateStbR | (double) The value (in Ohms) of any stabilization resistors on the gate of the DUT. The software automatically compensates for this resistor (based on the setting of GateStabilityResType). |
| GateStbRType | (int) Specifies the type of stabilization resistor used on the DUT Gate. There are 2 types of resistors. A series resistor is connected in-line between the pulse source and the gate. A parallel resistor is connected between the gate and ground (coax shield).<br>0 = no stabilization resistor<br>1 = Series resistor<br>2 = Parallel, or shunt, resistor |
| DrainStbR | (double) The value (in Ohms) of any stabilization resistors on the drain of the DUT. The software automatically compensates for this resistor (based on the setting of DrainStbResType). |
| DrainStbRType | (int) Specifies the type of stabilization resistor used on the DUT Drain. There are 2 types of resistors. A series resistor is connected in-line between the pulse source and the drain. A parallel resistor is connected between the drain and ground (coax shield).<br>0 = no stabilization resistor<br>1 = Series resistor<br>2 = Parallel, or shunt, resistor |
| MaxIg | (double) The max current allowed for the DUT Gate, for both DC and pulse. If the Gate current becomes greater than MaxIg, the test will exit and output a |

| | |
|---|---|
| | message to the KITE Project Message window. MaxIg value is also used to set Gate SMU current compliance. |
| MaxId | (double) The max current allowed for the DUT Drain, for both DC and pulse. If the Drain Current becomes greater than MaxId, the test will exit and output a message to the KITE Project Message window. MaxId value is also used to set Drain SMU current compliance. |
| MaxPowerGate | (double) The max power allowed for the DUT Gate. If the sourced power becomes greater than the MaxPowerGate, the test will exit. Maximum pulse output power:<br>GateVPURange = 5V: 5V x 100 mA = 0.5W<br>GateVPURange = 20V: 20V x 400 mA = 8W |
| MaxPowerDrain | (double) The max power allowed for the DUT Drain. If the sourced power becomes greater than the MaxPowerDrain, the test will exit. Maximum pulse output power:<br>DrainVPURange = 10V: 9.5V x 190 mA = 1.8W<br>DrainVPURange = 40V: 38V x 760 mA = 28.8W |
| NPLC | (double) The DC measurement integration time in NPLC (Number of Power Line cycles). |
| DCSourceDelay | (double) Time, in seconds, between the DC source and measure for each sweep point. |
| DC_vs_Pulse | (int) Determines whether to run a DC & Pulse test or a DC only test or a Pulse only test.<br>0 - Pulse Only<br>1 - DC Only<br>2 – DC, then Pulse. |
| GateSMU | (char*) String representing the ID for the SMU connected to the DUT Gate. Example: "SMU1" (do not include quotes). |
| DrainSMU | (char*) String representing the ID for the SMU connected to the DUT Drain. Example: "SMU2" (do not include quotes). |
| GateVPU | (char*) String representing the ID for the PG2 connected to the DUT Gate. This is usually the PG2 in the right most, lowest numbered slot. Example: "VPU1" (do not include quotes). (See Figure 7) |
| DrainVPUHigh | (char*) String for one of two VPU cards connected to the 4205-PCU for the DUT Drain. This is the card on the right (or the card with the lower ID number), when facing the back of the 4200 system. Example: "VPU2" (do not include quotes). (See Figure 7) |
| DrainVPULow | (char*) String representing the lower VPU on the 4205-PCU for the DUT Drain. This is the card on the left (or the card with the higher ID number), when facing the back of the 4200 system. Example: "VPU3" (do not include quotes). (See Figure 7) |
| DrainV_DC_X_Size<br>DrainI_DC_X_Size<br>GateV_DC_X_Size<br>GateI_DC_X_Size | (int) Sizes of the output arrays. Note that all arrays must be the same size and need to be large enough to hold all sweep points. |

DrainV_Pulse_X_Size
DrainI_Pulse_X_Size
GateV_Pulse_X_Size
GateI_Pulse_X_Size

PostData (int) Determines whether data is returned and plotted real-time.
0 = data returned and graphed after completion of test
1 = data returned and graphed real-time during test

## Running QPulseIV-Complete or Demo-QPulseIV for the first time

1. Connect the 4200-PIV-Q as documented above, using Figures 6-9.
2. If KITE is not running, start KITE by double-clicking the KITE icon on the 4200 desktop.
3. Open the 4200 Project, either QPulseIV-Complete (on-wafer) or Demo-QPulseIV (Demo DUT in 8101-PIV test fixture (Figure 9)):
    a. QPulseIV-Complete: Within KITE, click FILE > Open Project. If not in the _Pulse folder, move up one level to the display the Projects directory. Double-click the "_Pulse" folder, then double-click the QPulseIV-Complete folder, then double-click the QPulseIV-Complete.kpr file.
    b. Demo-QPulseIV: Navigate to the _Demo folder, then double-click Demo-QPulseIV folder, then double-click Demo-QPulseIV.kpr file.
4. The screen should resemble the screen shot in either Figure 17 (Demo-QPulseIV) or Figure 18 (QPulseIV-Complete). The right portion of the screen may not be the graph shown, but the project navigator (left side "tree" in window) should match that shown in Figure 17 or 18.
5. Connect or touch-down on the chosen device under test (DUT).
6. Verify setup.
    a. Step 1: Follow the instructions for "Running ScopeShot-FET" to validate proper setup and operation of the PIV-Q package. Ensure that both the gate and drain waveforms are visible and do not have any significant ringing or overshoot.
    b. Step 2: Try running Vd-Id-Pulse ("Running Vd-Id-Pulse") and/or Vg-Id-Pulse ("Running Vg-Id-Pulse") and look for a characteristic response. If desired, DC IV tests may also be run ("Running Vd-Id-DC", "Running Vg-Id-DC"). Once both the scope-shot and a pulse IV test have been verified, Cable Compensation (pulse system calibration) can be performed.
7. Calibration: Follow "Running AutocalScope" and "Running PulseIVCal" in this document to perform the necessary pulse calibrations.
8. Use: After successful pulse calibrations, the system is now ready to be used for pulse and DC characterization of transistor devices.

### Running AutocalScope

AutocalScope should be run before any pulse calibration is performed. For best Pulse IV results, the AutocalScope should also be run before the first experiments of the day.

1. The 4200-SCS should be turned on at least 30 minutes before performing any calibration or measurements.
2. Double-click AutocalScope in the Project Navigator (Figure 17 or 18).
3. Click the green Run button.
4. Follow the instructions given on the pop-up dialog box (Figure 20) and disconnect all connections to the 4200 Scope card.
5. The SCP2HR performs an autocal, which takes about 2 minutes.
6. The test is complete when the Run button is green. In the Sheet tab, an AutoCalStatus=0 means that there were no errors.

7. Reconnect the cables to the 4200-SCP2HR. Use care when installing the cable to the 4200-SCP2HR trigger SMB connector.

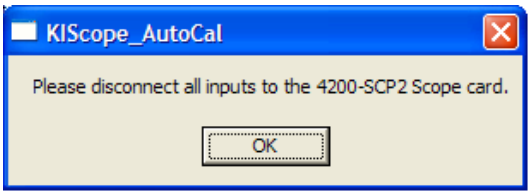


***Figure 20.*** *AutocalScope Dialog box.*

## Running Cable Compensation for Pulse IV

Verify proper setup by running a ScopeShot. For on-wafer testing, have a through, or short, structure available, or ensure that sharing a pad for both the gate and drain probes provides a good connection. There are three steps to the calibration, open, through, and a second open.

1. If not already performed, run the AutocalScope procedure.
2. Double-click CableCompensation on the Project Navigator.
3. Click the green Run button to start the CableCompensation Cal.
4. Click OK on the first dialog box to continue the CableCompensation (Figure 21a, left dialog box).
5. The second dialog box requests that the probe pins be raised from the wafer, breaking contact. Raise probe pins or lower wafer to create the Open condition.
6. Click OK on the Open dialog box. The Open portion should take much less than 1 minute.
7. The third dialog box requests that the probe pins be connected to each other via a through device. Lower the probes onto a through device.
8. Click OK on the Through dialog box. The Through portion should take about 2-3 minutes.
9. Click OK on the Open 2 dialog box. This portion should take about 15-20 minutes.
10. The test is complete when the Run button is green. In the Sheet tab, a cal_pulseiv=0 implies that there were no errors.
11. The system is now ready to test regular devices.

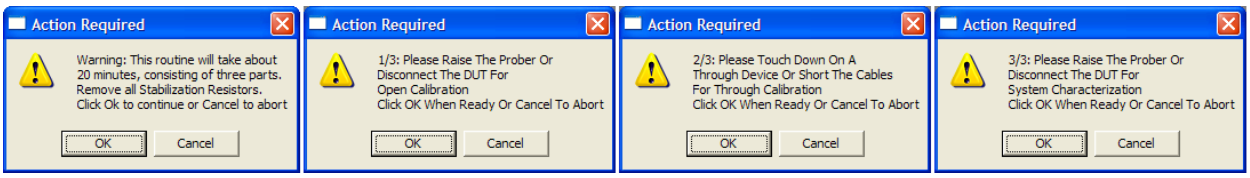


***Figure 21a.*** *Dialog boxes for Cable Compensation: Information, Raise probes, Touch down on through structure, Raise probes.*

## Running Measure_Stability_Resistance

This test is located in the Initialization Steps portion on QPulseIV-Complete (Figure 18). It is an optional routine, as the resistance values for the stability resistors in the 4200-Q-STBL-KIT are accurate to 0.1% and will not benefit from a SMU measurement of the resistance.

1. Disconnect SMA cabling from the probes
2. Enter the appropriate value for ResType:
    a. ResType = 1 for Series stability resistor
    b. ResType = 2 for Parallel, or shunt, stability resistor
3. Click the green Run button to run the Measure_Stability_Resistance.

4. Follow the instructions given on the pop-up dialog box and connect the stabilization box to the gate and drain SMA cables.
    a. Series stability resistor - It does not matter which cable is attached to which side of the stabilization box (Figure 21b).
    b. Parallel stability resistor – Just connect the gate SMA cable to one of the connectors on the resistor box (Figure 21c). The drain SMA cable should not be connected to the resistor box.


***Figure 21b.*** *Dialog box for measuring a series stability resistor.*


***Figure 21c.*** *Dialog box for measuring a parallel stability resistor.*

**Determining the settings for the Bias, or Q-, Point**

The desired bias point is usually supplied as a $V_D$ and $I_D$. Therefore, the $V_G$ that corresponds to this $V_D$ & $I_D$ combination needs to be determined. If a non-zero bias point is not required, just set $V_G$ Q-point and $V_D$ Q-point to 0V.

1. Touch down on the DUT
2. Set the initial Qpoint values to ensure the DUT is off in between each pulse:
    a. For enhancement mode devices
        i. VgQPoint = 0V
        ii. VdQPoint= 0V
    b. For depletion mode devices
        i. VgQPoint = -nV, where -n is large enough to ensure device is off without causing damage to the DUT
        ii. VdQPoint= 0V
3. Verify proper connection by running a ScopeShot-FET test, using parameter values that will not cause damage to the DUT.
4. The easiest way to determine the $V_G$ for the corresponding $V_D/I_D$ combination is to perform a $V_G$-$I_D$ test. Run a $V_G$-$I_D$ curve. Ensure that the power and current limits are set for the drain. Then just read the appropriate $V_G$ from the X axis.
5. Check for oscillation. Use ScopeShot-FET to view a pulse from an off condition q-point to the bias point condition determined above. Ensure that pulse shape is acceptable and no oscillations occur (see Determination of oscillation). The voltages corresponding to the off condition depend on the type of device.
    a. For enhancement mode devices: $V_G$ = 0V, $V_D$ = 0V

b. For depletion mode devices: $V_G$ = -2V to -5V, $V_D$ = 0V.
Ensure that the device is off by using a fairly negative $V_G$, but not so negative as to cause damage or breakdown.

**Running Vd-Id-DC, Vd-Id-Pulse or Vd-Id-Family**

Vd-Id-DC
Vd-Id-Pulse
Vd-Id-Family

These routines perform a Vd-Id sweep and are included with Demo-QPulseIV (Figure 17) and QPulseIV-Complete (Figure 18). Only the Vd-Id-Family test performs multiple sweeps, of either DC, pulse IV or DC and pulse IV. The values given below are starting values, adjust to match DUT behavior and desired results.

Note that the Demo-QPulseIV has GateSMU = SMU2 and DrainSMU = SMU3, which may not match a typical 4200-SCS chassis. Please change these defaults to match the system interconnect used above. QPulseIV-Complete has GateSMU = SMU1 and DrainSMU = SMU2

1. Pick the desired Vd-Id test by double-clicking the test in the Project Navigator panel on the left.
2. Enter the desired values for $V_G$, $V_D$ start, stop and step size.
3. Suggested values for DC parameters:
    a. GateRange = 7, limited autorange starting with the minimum range of 1 uA (1 pA resolution)
    b. DrainRange = 7, limited autorange starting with the minimum range of 1 uA (1 pA resolution)
    c. NPLC = 1
    d. DCSourceDelay = 0.005
4. Suggested values for Pulse parameters
    a. PulseWidth = 2 us, but use any pulse width desired from 500 ns to 999 ms
    b. PulsePeriod = 100 us, which results in a 2% duty cycle
    c. RiseTime = 150 ns
    d. FallTime = 150 ns
    e. PulseAverage= 50
        i. Use 10-30 for 100 us – 500 us
        ii. Use ≤5 for PW ≥1 ms
    f. GateVPURange = 5
        i. Use 20 for Vg > 10V or for DUTs with Ig > 50 mA
    g. DrainVPURange = 40
        i. Use 10 for lower power DUTs (see Table 5 for maximum Vd and Id values) and to reduce the offset for Vd near 0V.
    h. GateScpRange = 0, autorange, which will provide the best $V_G$ and $I_G$ results
        i. Or specify a fixed range to decrease test time, which may degrade $I_G$ measurement performance. If a signal is too large for a given fixed range, the system will respond with a “Gate Source OVERV” message in the Project Messages window and the test will end.
            1. 5, for $V_G$ < ±1.6V
            2. 10, for $V_G$ < ±3.5V
            3. 25, for $V_G$ < ±9V
            4. 50, for maximum $V_G$ of ±20V
    i. DrainScpRange= 0, autorange, which will provide the best $I_D$ results
        i. Or specify a fixed range to decrease test time, which will degrade $I_D$ measurement performance
            1. 0.5, for $I_D$ < ±0.035A and $V_D$ < ±8V
            2. 1.25, for $I_D$ < ±0.09A and $V_D$ < ±25V
            3. 2.5, for $I_D$ < ±0.180A and $V_D$ < ±50V

4. 5, for $I_D$ < ±0.36 A and $V_D$ < ±75V
5. 10, for $I_D$ < ±0.72 A and $V_D$ < ±75V
6. 25, for $I_D$ < ±1.5 A and $V_D$ < ±75V

j. QPointLoadLine = 1, enabling Load Line Compensation when applying the Q-point voltages
   i. Using 0 is not recommended, but may be useful in unusual cases. With Load Line disabled, the voltages requested for $V_G$ and $V_D$ are output by the pulse hardware, without regard to DUT impedance, which can result in DUT voltages much higher, or lower than expected. Even if the q-point voltages are set to 0V, it is usually desired that the voltages at the DUT are as close as possible to 0V, which requires QPointLoadLine = 1.

k. GateLoadLine = 1, enabling Load Line Compensation when applying $V_G$, applies to both DC and pulse IV
   i. 0 will disable Load Line Compensation for the Gate. Generally, there is little benefit to disabling Load Line Compensation on the gate. Disabling Load Line Compensation for the gate will result in the requested $V_G$ being output by the Gate VPU, which will result in the actual $V_G$ at the DUT to double if the gate is high impedance.

l. DrainLoadLine = 1, enabling Load Line Compensation when applying $V_D$, applies to both DC and pulse IV
   i. 0 will disable Load Line Compensation for the Drain. Disabling Load Line Compensation for the drain is necessary when the Load Line Compensation algorithm cannot match the behavior of a high gain DUT. See Troubleshooting section for when and how to address this situation. Disabling Load Line Compensation for the drain will result in the requested $V_D$ being output by the Drain VPU, which will result in the actual $V_D$ at the DUT to be different, depending on drain-source impedance.

m. LL_Iterations = 50, applies to both DC and pulse IV
   i. A smaller value for LL_Iterations will result in shorter test times, especially when testing a high gain device or when the PulseAverage or number of sweep steps is high. But, the spacing of the resulting $V_D$ will not be as close to the desired $V_D$ step size.
   ii. A higher value, up to 200, is appropriate for rapidly changing $I_D$ signals, such as high gain transistors in the linear region of a $V_D$-$I_D$ curve. Also use a larger value when the voltage difference between VdQPoint and the first point of a Vd sweep is large.

n. OffsetCorrect = 1, which is appropriate for almost all test.
   i. 0 turns off OffsetCorrect, and is used for troubleshooting by experienced personnel or applications engineers.
   ii. 2 is similar to OffsetCorrect = 1, but uses scope offset measurements taken at the start of the test as part of the offset correct algorithm, which may provide results with less run-to-run variation, but at the expense of an additional 30-40 seconds for each sweep.

o. GateStbR = xxx, use appropriate value
   i. Using a stability resistor is only necessary to address oscillation when testing RF transistors. See "Determining and Addressing Oscillation for RF Transistors" section.
   ii. To disable software correction for stability resistor, see

p. GateStbRType = 0, when no stabilization resistor is connected to the DUT gate
   i. 1, when using a series stabilization resistor on the gate (typical)
   ii. 2, when using a parallel stabilization resistor on the gate (unusual)

q. DrainStbR = xxx, use appropriate value
   i. Using a stability resistor is only necessary to address oscillation when testing RF transistors. See "Determining and Addressing Oscillation for RF Transistors" section.
   ii. To disable software correction for stability resistor, see

r. DrainStbRType = 0, when no stabilization resistor is connected to the DUT drain
    i. 1, when using a series stabilization resistor on the drain (unusual)
    ii. 2, when using a parallel stabilization resistor on the drain (typical)
s. MaxIg = 0.100, or set to desired max gate current for the DUT, applies to both DC and pulse IV.
t. MaxId = 1.33, or set to desired max drain current for the DUT, applies to both DC and pulse IV.
    i. See "Maximum Voltage and Current for the Drain and Gate" section, especially Table 5 for expected $V_D$ and $I_D$ for particular $R_{DS}$ values.
u. MaxPowerGate = 5, , or set to desired max gate power for the DUT, applies to both DC and pulse IV.
v. MaxPowerDrain = 28, or set to desired max drain power for the DUT, applies to both DC and pulse IV
w. GateSMU = SMU1, or set to desired SMU number. SMU numbers start at the right-most slot, when looking at the back of the 4200-SCS chassis. Note that Demo-QPulseIV has GateSMU = SMU2.
x. DrainSMU = SMU2, or set to desired SMU number. SMU numbers start at the right-most slot, when looking at the back of the 4200-SCS chassis. Note that Demo-QPulseIV has DrainSMU = SMU3.
y. GateVPU = VPU1, VPU card numbers start at the right-most slot, when looking at the back of the 4200-SCS chassis. The VPU in the lowest numbered slot (counting from the right) is VPU1. This default value is appropriate for almost all 4200-SCS chassis configurations.
z. DrainVPUHigh = VPU2, VPU card numbers start at the right-most slot, when looking at the back of the 4200-SCS chassis. The VPU in the lowest numbered slot (counting from the right) is VPU1, with additional PG2 cards to the left numbered VPU2, VPU3, etc.
aa. DrainVPULow = VPU3, VPU card numbers start at the right-most slot, when looking at the back of the 4200-SCS chassis. The VPU in the lowest numbered slot (counting from the right) is VPU1, with additional PG2 cards to the left numbered VPU2, VPU3, etc.
bb. DrainVSize, DrainISize, GateVSize, GateISize, etc = 1000, or set all size parameters to the desired maximum number of points in the sweep. Note that all size parameter values must be > number of sweep points, and all sizes must be set the same value.
cc. PostData = 1, data returned and graphed real-time during test. Note that the multi-sweep tests (Vd-Id-Family and Vg-Id-Pulse-vs-DC) do not return data or graph real-time.

**Running Vg-Id-DC, Vg-Id-Pulse or Vg-Id-Pulse-vs-DC**

Vg-Id-DC
Vg-Id-Pulse
Vg-Id-Pulse-vs-DC

These routines perform a Vg-Id sweep and are included with Demo-QPulseIV (Figure 17) and QPulseIV-Complete (Figure 18). The Vg-Id-Pulse-vs-DC test performs either DC, pulse IV or DC and pulse IV. The parameters in these tests are similar to Vd-Id, only the unique parameters are listed below. The values given below are starting values, adjust to match DUT behavior and desired results.

1. Pick the desired Vg-Id test by double-clicking the test in the Project Navigator panel on the left.
2. Enter the desired values for $V_D$, $V_G$ start, stop and step size.
3. Look to "Running Vd-Id" above for suggested values for remaining parameters.

# Troubleshooting 4200-PIV-Q

Since testing of RF transistors is a bit tricky, there are many test parameters for each test. In addition, LDMOS transistors for switching power supplies have an overlapping set of test parameters. This permits maximum flexibility to obtain the best possible results, but also increases the chance of improper configuration.

## Determining and Addressing Oscillation for RF Transistors

Oscillation is caused by the undesirable amplification of particular signals due to feedback paths. As discussed above, this is addressed by adding stabilization resistors to reduce the loop gain and retard the oscillation. Conditions that cause oscillation can be specific to the device, cabling, test voltage or even the bias point settings. Oscillation is fairly common for compound semiconductor RF transistors. Determining oscillation is done by the user, using at least one of the methods described below.

Is there oscillation?

1. Experienced user can look at a family of curves and note oscillation areas as deviations from the expected characteristic response. An example of relatively small deviations is shown in Figure 22.
2. ScopeShot waveforms can also be used. Figure 23 shows oscillation on the $I_D$ curve. This is just one example, the oscillations may be more subtle, showing undesirable undulations where the pulse top should be flat, or more severe, where the entire pulse waveform shows oscillation (Figure 24).

It is important to note that Figure 22 indicates that the other curves, or even other portions of curves where the deviations occur, are probably not oscillating. In reviewing of the results shown in Figure 22, the user may decide that the results are acceptable and post-processing of the data will be utilized. If the ScopeShot results shown in Figure 23 or 24 are seen using sweep conditions, then steps must be taken to reduce or eliminate the oscillation.

Addressing oscillation

Addressing oscillation is an iterative process. Once a certain amount of experience is developed on a device type, it may be possible to develop a general approach. Note that adding stabilization resistor(s) can have a significant effect on the Q-point. So after each change in a stabilization resistor value, verify the Q-point values.

1. First, break contact with the device by lifting probes or lowering platen.
2. Carefully disconnect and remove the SMA barrel from the short cable attached to the gate side.
3. Insert a series resistor. Start with a smaller series resistor (100-500 Ω), minimizing the stress on the probe connection.
4. Modify the parameters in the desired test.
    a. The parameters for the gate:
        i. GateStbR: Set it to the value used, in Ω. Note that the stability resistors are 0.1%, so the value on the box is within 0.1% of the actual resistance value.
        ii. GateStbRType: Set this value to 1, for series resistance. After replacing a resistor box with the SMA barrel, set this parameter = 0.
    b. The parameters for the drain
        i. DrainStbR: Set it to the value used, in Ω. Note that the stability resistors are 0.1%, so the value on the box is within 0.1% of the actual resistance value.
        ii. DrainStbRType: Set this value to 2, for shunt resistance. After replacing a resistor box with the SMA barrel, set this parameter = 0.

5. Run the test. If using $V_D$-$I_D$, then run the curve(s) that previously showed the effect. If using ScopeShot, run another pulse, making sure that the PulseAverage = 1, so that any oscillation is not "averaged" away. The oscillation will be at a high frequency, which will be aliased on the scope shot view.
6. If the oscillation is removed, then check the Q-point. Stabilization resistors will typically shift the operating point of the device.
    a. Use ScopeShot-FET. Set the $V_G$ and $V_D$ values to the Q-point values determined previously. Set the Q-point values to ensure the DUT is off in between the pulses (see "Determining the settings for the Bias, or Q-, Point," above).
    b. Compare the reported measurements for $V_G$, $I_G$, $V_D$ and $I_D$. Note that these values are in the sheet tab for all test runs, and the first run (called "Data") is shown on the lower left of the ScopeShot graph (Figure 13). If using the Append to perform tests, ensure that the latest append tab is being used for the results comparison.
7. If the oscillation is not retarded sufficiently, there are two possible paths
    a. Keep the existing series resistor on the gate, and add a high resistance parallel resistor to the drain. In general, it is preferred to use just the series resistance on the gate, as adding parallel resistance to the drain means that there is less current available for the DUT.
    b. Increase the resistance of the series resistor on the gate.
    c. For subsequent passes:
        i. Increase series Ω on gate or
        ii. Reduce parallel Ω on the drain.
8. Install the new stabilization resistor, using the approach outlined in steps 1, 3 & 4 above.
9. Re-run the test as described in steps 5-6.
10. Continue steps 1-9 until an acceptable response is obtained.

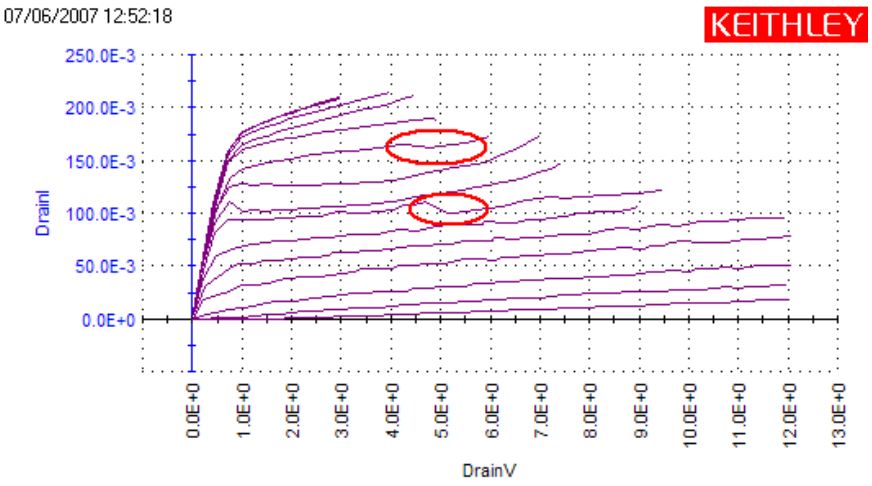


***Figure 22.*** *Pulse $V_D$-$I_D$ family of curves, with circles areas showing deviations possibly caused by oscillation.*

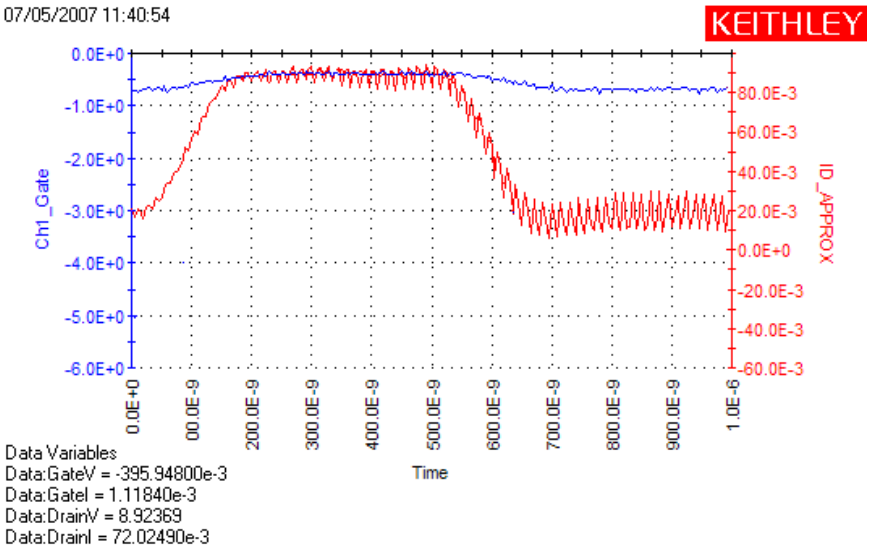


**Figure 23.** Pulse waveform, from ScopeShot-FET, showing oscillation on the red $I_D$ curve.

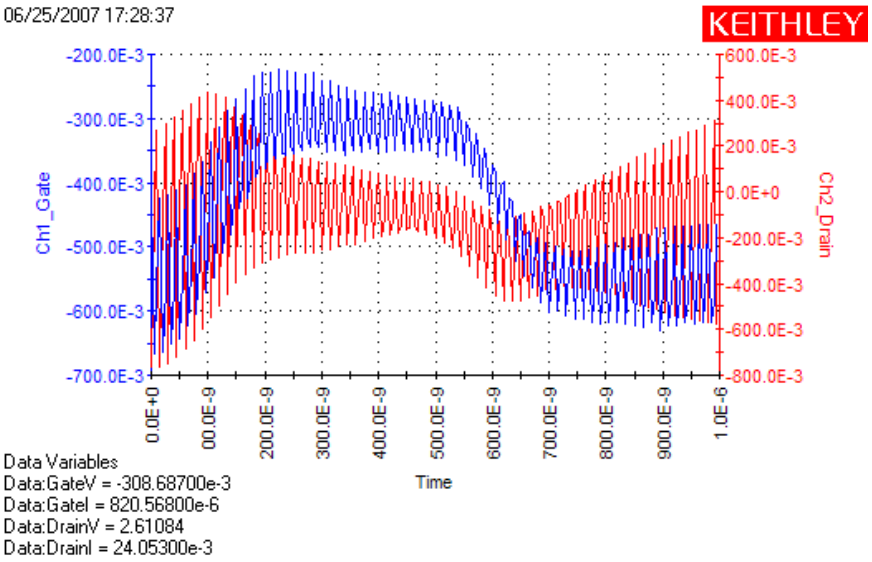


**Figure 24.** Pulse waveform, from ScopeShot-FET, showing significant oscillation on both the blue $V_G$ and red $I_D$ curves.

## Load Line Compensation "zigzag" Behavior in $V_D$-$I_D$

On certain high gain DUTs, the Load Line Compensation algorithm interacts with the DUT behavior results in a "zigzag" Vd-Id curve as shown in Figure 25. This is most likely when there is a high gain device and/or there is a fairly sharp transition from the linear to saturation portion of the $V_D$-$I_D$ curve.

- Disable Drain Load Line Compensation
  - DrainLoadLine = 0
- Determine approximate pulse source voltage required
  - Disabling Drain Load Line compensation means that the values specified for $V_D$ need to be "manually" increased to account for the Load Line effect and get a $V_D$ that is close to the desired voltages.

- Equation to estimate the pulse source voltage for $V_D$.
    1. No Load Line Compensation $V_D$ = [(Max $V_D$ desired) + (Max $I_D$) x (55 + $R_{INTERCONNECT}$)] / 2
    2. $R_{INTERCONNECT}$ is the estimated resistance of the interconnect; a typical range for on-wafer testing is 3-7 Ω.
    3. The above equation is the desired drain voltage, plus additional voltage that is the Load Line effect (estimated)
    4. This equation is included in Vd-Id-Pulse test in QPulseIV-Complete in Formulator. This may provide a good starting point for the $V_D$, assuming that the curve began to zigzag at a point near the maximum $I_D$, as shown in Figure 25. The resulting value is in the right-most column of the Sheet (Figure 26).

- If the maximum power for the drain is know, enter it before running the Vd-Id test.
    - Once the DUT reaches the saturation region, $R_{DS}$ changes rapidly, so the final DUT $V_D$ is a function of the sourced $V_D$ reacting to $R_{DS}$.
- Input first estimate of $V_D$ and run Vd-Id test, then manually iterate value to reach desired DUT $V_D$.
    - If there is any doubt in the calculation, subtract 1-2V from the calculation before entering it.
    - Try ever increasing value for $V_D$, noting that even a 0.1V shift in the sourced $V_D$ can cause a several volt shift in the DUT $V_D$.

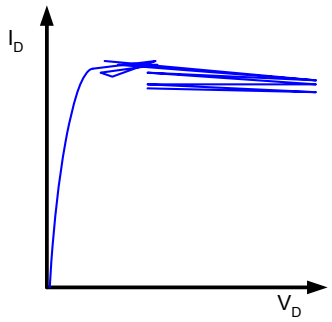


***Figure 25.*** *Example of Load Line Compensation zigzag effect.*

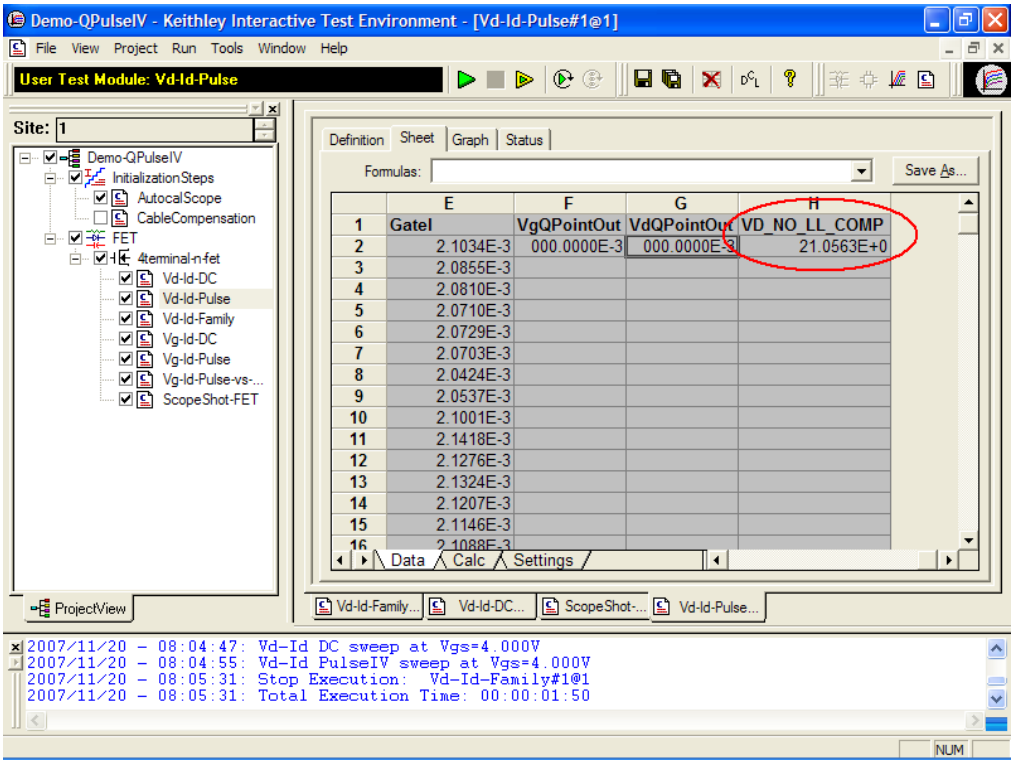


***Figure 26.*** *Result of $V_D$ calculation for Drain Load Line Compensation off.*

**"Gate Measurement Overvoltage on GateScpRange = nnV"**
**"Drain Measurement Overvoltage on DrainScpRange = nnV" in KITE Project Messages Window**

The pulse waveform did not fit within the scope measurement range.

- If using a fixed range, for GateScpRange or DrainScpRange, try the next larger range (listed in the Help window).
- If using auto-range for both GateScpRange and DrainScpRange, there may be oscillation, or some other test instability
    - Try using large fixed ranges for both the gate and drain
        - GateScpRange = 50
        - DrainScpRange = 50
    - If the test completes, then the results may indicate the problem with the test.
        - May have oscillation
            - Use ScopeShot to verify, as directed in "Determining and Addressing Oscillation for RF Transistors"
            - If oscillation seems likely, implement stabilization resistors as directed in "Determining and Addressing Oscillation for RF Transistors"
        - If running $V_D$-$I_D$, try a lower setting for $V_G$ to verify DUT operation
    - If the test still stops with the same error, after setting ranges to largest fixed range
        - May have oscillation
            - Use ScopeShot to verify, as directed in "Determining and Addressing Oscillation for RF Transistors"

**"Maximum source voltage reached on GateVPURange = nnV"**
**"Maximum source voltage reached on DrainVPURange = nnV" in KITE Project Messages Window**

This message is output when using Load Line Compensation for the Gate or Drain, respectively, and the pulse source is attempting the maximum possible voltage to compensate for the load line effect. The system responds by outputting this message for every point in the sweep where the condition occurs, similar to SMU compliance.

- The pulser will continue to output the maximum value, and the test will continue until the desired number of sweep points is completed.
  - All remaining graph points will be nearly coincident.
  - See Figure 27.
- Try the highest range for the pulser
  - GateVPURange = 20
  - DrainVPURange = 40
  - See section “Maximum Voltage and Current for the Drain and Gate”, specifically Tables 6 and 7.
  - If the desired value is greater of the data given above, then the 4200-PIV-Q system is at its source maximum and cannot provide additional pulsing voltage or current.
- If stabilization resistors are used, note the following
  - Gate
    - Series stabilization resistors result in less voltage at DUT gate, which may cause this error
  - Drain
    - Parallel stabilization resistors result in less current flowing through the DUT drain, which may cause this error

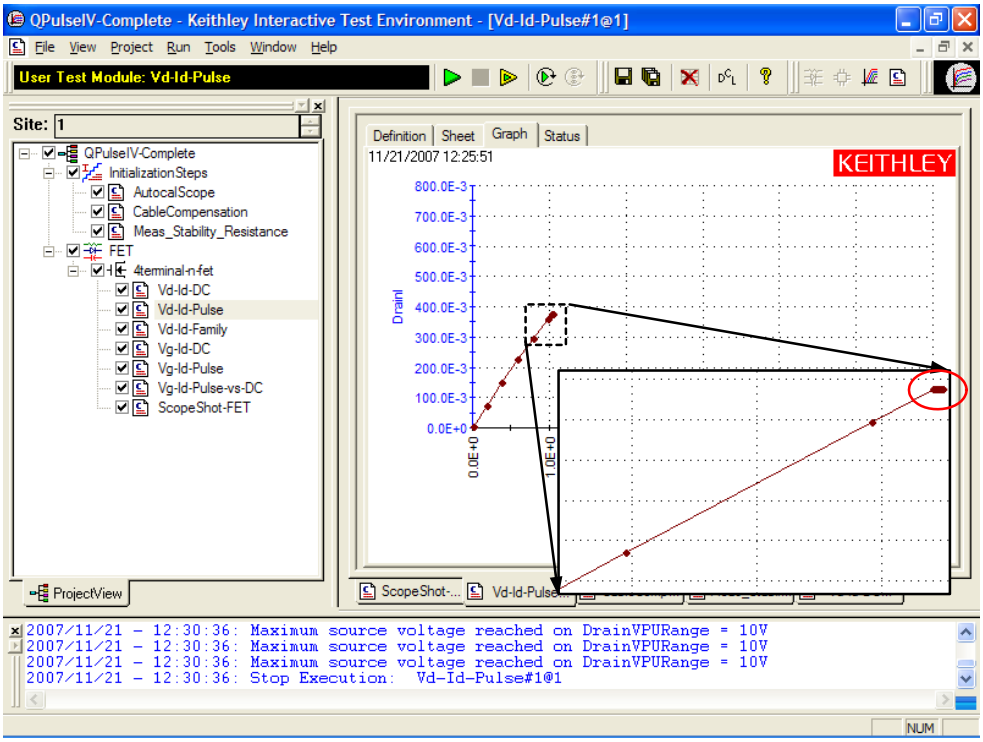


***Figure 27.*** *$V_D$-$I_D$ curve where the maximum drain voltage was reached. Note the red oval, marking all of the coincident points once the Drain VPU source had reached maximum output.*

**ERROR – Vg_Id_Single_DC_QPulseIV (Vds=n.nnV) Max Id reached**
**ERROR – Vd_Id_Single_Pulse_QPulseIV (Vgs=n.nnV) Max Id reached**
**ERROR – Vd_Id_Single_Pulse_QPulseIV (Vgs=n.nnV) Max Drain Power reached**
And similar

- These messages are output only into the KITE Project Messages window
- Once the condition is met, the sweep is stopped. Multi-sweep tests will continue to the next sweep.
- Note that these max current and power parameters are for the DUT and do not include the losses due to the stabilization resistors.

**Weird pulse shape - Incorrect SMU specified**

The 4200-PIV-Q requires 2 SMUs, as shown in Figure 1. The 4200-SCS chassis support more than 2 SMUs in the 4200-PIV-Q configuration. Figure 28 shows a scope-shot where the SMU was still connected to the pulse signal path, resulting from an incorrect value for the GATE and DRAIN.

- This means that the physical interconnect needs to match the specified SMUs in each of the QPulseIV tests.
    - Confirm the connection to SMUs and check the parameter settings
        - GateSMU
        - DrainSMU
    - For example, the physical configuration is using SMU1 and SMU2, but the SMU parameters in the tests are set to SMU2 and SMU3 (default case for all Demo-QPulseIV tests). This will result in the system switching the isolation relays, as shown in the SMU boxes at the middle of Figure 1, to the open state on SMU3 and SMU4. But, since SMU1 and SMU2 are the SMUs used, they will be connected during any pulse IV test, causing unexpected results.

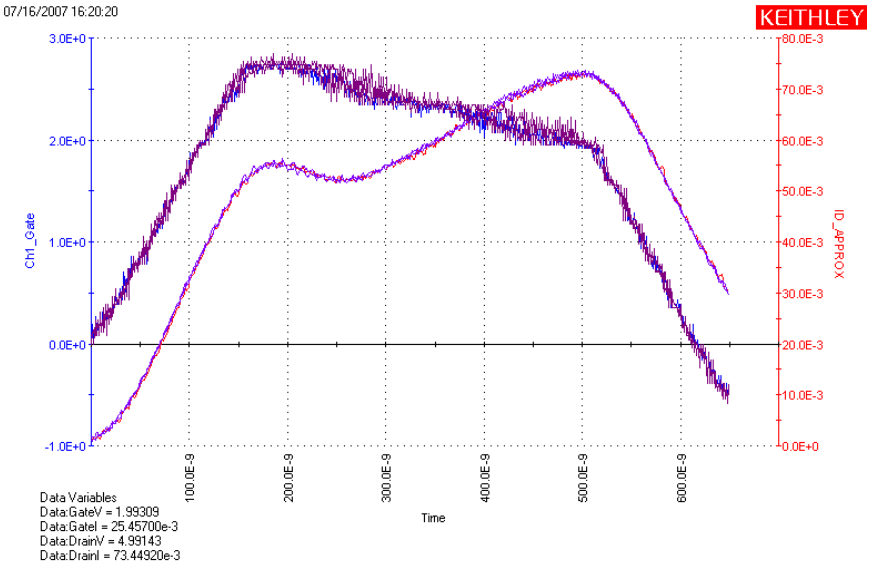


***Figure 28.*** *Scope-shot result with incorrect SMUs specified for the gate and drain.*

**Vd-Id curve shifted to the left (negative x-axis) or down (negative y-axis) - Old or incorrect Cable Compensation**

As described above, it is important to perform AutocalScope and Cable Compensation during initial setup, or after any interconnect changes. If not, the unexpected results may occur. Using an outdated cable compensation, obviously undesirable, would result in the reported current being less accurate than it

could be. This is true, but there is also an effect on the voltage supplied to the DUT, which can shift the curve to the left, as shown in Figure 29.

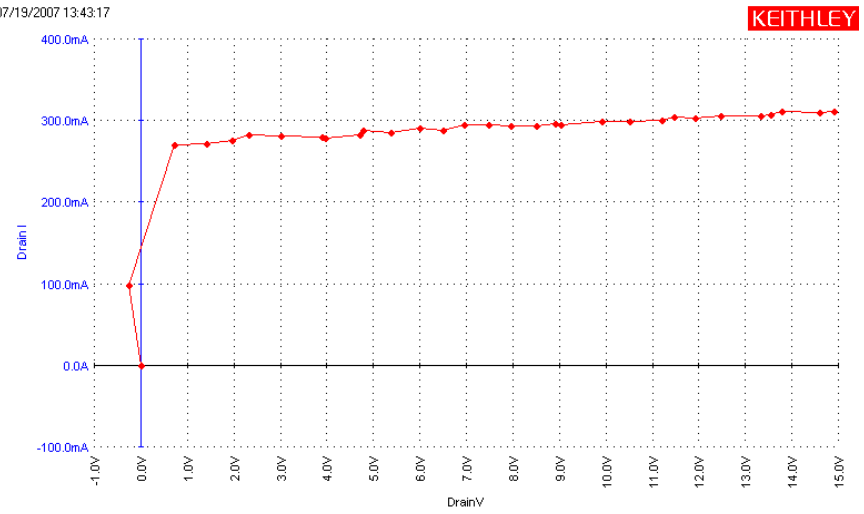


***Figure 29.*** *$V_D$-$I_D$ curve with outdated or incorrect Cable Compensation factors. Note that the curve is partially shifted to the left. Perform an AutocalScope and CableCompensation with the present setup, then re-run the test to obtain expected results.*

## Error Code Troubleshooting

-206 pulse_vhigh(): V-limit value x.xxxe+37 too large for specified range

There are a few possible configurations that may cause this error:

- Fixed scope range (GateScpRange or DrainScpRange) set too low for the desired test conditions. At some point during a sweep, the gate or drain signal will be too large, causing an overvoltage measurement and returning a ±x.xxe+37 value, which causes the test to stop. Fix: try a larger gate and/or drain range (max is 50V), or switch to auto-ranging the measurement (Range = 0). Note that autoranging adds test time.
- Oscillations causing overvoltage condition. This is similar to the fixed range issue, where an overvoltage condition is caused by a fixed range. However, in this case the overvoltage is caused by oscillation. See "Determining and Addressing Oscillation for RF Transistors" for more information.

## Tips for using Dual Channel Quiescent Point Pulse IV

- Confirm connection: Use ScopeShot as the first test after touching down on a device to confirm that there is proper connection to the DUT, *before* running CableCompensation or any pulse tests.
- Always run CableCompensation after any setup changes (new probe tips or manipulators, cable replacement)
- High gain RF devices are more likely to oscillate, requiring the use of the stabilization kit.
- Even after stabilization, some devices may have some portion of results that may be attributed to oscillation. In these cases, it may not be possible to eliminate this effect and post-processing of the data may be necessary.