# KTEI 6.2

**4205-PG2, 4200-SCP2, 4200-SCP2HR, 4200-PIV-A, 4200-PIV-Q, 4200-FLASH**

- **4205-PG2 pulse generator provides voltage pulses with periods as short as 20ns in high speed mode or up to ±20V (into 50Ω) in high voltage mode**
  - **Generate complex waveforms of up to 256K data points at sample rates up to 50MHz in ARB mode**
  - **Create and generate waveforms based on up to 1024 line segments with the patent-pending Segment ARB™ mode**
  - **Support for up to four dual-channel pulse generators (4205-PG2) in each 4200-SCS chassis to supply up to eight pulse generator channels (such as for parallel AC stress for stress/measure reliability testing)**
  - **Support for new pulse applications, including charge pumping, FLASH memory testing, clock generation for test vectoring and failure analysis, digital triggering for multi-pin device testing**
- **Support for 8-bit (4200-SCP2) and 16-bit (4200-SCP2HR) digital oscilloscopes**
- **Systems can be configured with a choice of three applications packages: 4200-PIV-A, 4200-PIV-Q, and 4200-FLASH**
- **Available as new systems or as factory upgrades to existing units**

# Hardware/Software Upgrades and Pulse Applications Packages for the Model 4200-SCS


Version 6.2 of the Keithley Test Environment Interactive (KTEI) offers support for a variety of new hardware options and applications packages, further expanding the capabilities of Keithley's Model 4200-SCS, the industry's leading interactive semiconductor characterization system. These options can be included with new systems or as factory upgrades to existing units.

## New Dual-Channel Pulse Generator

The Model 4205-PG2 Dual-Channel Pulse Generator integrates pulsing with the Model 4200-SCS's DC source and measure capabilities. The pulse generator provides voltage pulses with periods as short as 20ns in high speed mode or up to ±20V (into 50Ω) in high voltage mode. This new instrument is designed as a replacement for the system's original pulse generator option, the Model 4200-PG2, adding an Arbitrary Waveform Generator mode and a Segment ARB™ Waveform mode (patent-pending).

The Arbitrary Waveform mode allows generating complex waveforms at sample rates up to 50MHz with a memory depth of 256K data points. The Segment ARB™ mode allows for easy creation and generation of complex waveforms using line segments defined by their start and stop voltages and duration. The 4205-PG2 can store and generate Segment ARB™ waveforms made up of up to 1024 segments.

Other new features include the ability to install up to four pulse generators in one Model 4200-SCS chassis, a trigger-in capability to allow for external triggering (useful for synchronizing multiple pulse generators), and an in-line High Endurance Output Relay (HEOR), which is useful for FLASH memory testing.

Installing one or more Model 4205-PG2 pulse generators in the Model 4200-SCS chassis expands the system's range of applications significantly, including:

- Charge pumping (including tri-level charge pumping) for interface charge trap characterization
- Up to eight channels of pulse for parallel AC stress for stress/measure reliability testing
- Flash memory testing
- Clock generation for test vectoring and failure analysis
- Digital triggering for multi-pin device testing

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# KTEI 6.2

**4205-PG2, 4200-SCP2, 4200-SCP2HR, 4200-PIV-A, 4200-PIV-Q, 4200-FLASH**

# Hardware/Software Upgrades and Pulse Applications Packages for the Model 4200-SCS

The Model 4205-PG2 comes with a variety of User Test Modules (UTMs) that make it easy to incorporate the pulse generator into Keithley Interactive Test Environment (KITE) test sequences. The Graphical User Interface supplied with the pulse generator (KPulse) allows driving it as a stand-alone pulser or wave generator for maximum flexibility and ease of use. The GUI supports all three modes of operation (Pulse, ARB, and Segment ARB™) and a wide range of operating variables, including pulse frequency, duty cycle, rise/fall time, amplitude, and offset, as well as the ability to trigger single pulses and/or pulse trains. The KPulse GUI can create complex waveforms in both the ARB and Segment ARB™ operating modes.

## Digital Oscilloscope

KTEI 6.2 supports either of two integrated digital oscilloscopes: the 8-bit Model 4200-SCP2 with a sample rate up to 2.5GS/s (one channel interleaved) and the 16-bit Model 4200-SCP2HR with a sample rate up to 400MS/s (also one channel interleaved). Both oscilloscopes offer general purpose scope capabilities and time-domain measurements to complement the pulser's time-domain sourcing. The scopes can be programmed for automated measurement and data acquisition or used with the stand-alone GUI (KScope) designed for performing traditional oscilloscope tasks. The scope makes measurements in both the time (frequency, rise/fall time) and voltage domains (amplitude, peak-peak, etc.).

## Applications Packages

By combining specific sets of hardware with Keithley-developed code and interconnect, a variety of applications packages are offered for specific test needs. These include the 4200-PIV-A package for charge trapping and isothermal testing in lower power technologies like CMOS, the 4200-PIV-Q package for higher power pulse testing in III-V and other higher frequency FET devices, and the 4200-FLASH package for testing FLASH memory devices (NOR and NAND, including MLC technologies). Table 1 provides an overview of the capabilities of each of the packages.

**Table 1. KTEI 6.2-supported applications packages.**

| | 4200-PIV-A | 4200-PIV-Q | 4200-FLASH |
|---|---|---|---|
| **Device** | FET | HEMT, FET | Floating gate FET |
| **Technology** | Advanced CMOS | III-V/LDMOS | NAND, NOR non-volatile memory |
| **Source Method** | Pulse gate, DC bias on drain | Dual pulse for gate and drain with quiescent point testing | Pulse gate, drain, source and substrate |
| **Measure Method** | Pulse I-V and DC | Pulse I-V and DC | DC only |
| **Measurements** | Gate voltage, drain voltage and current | Gate voltage and current, drain voltage and current | Gate voltage and current, drain voltage and current |
| **Pulse Width Range**[1] | 40ns to 150ns | 500ns to 999ms | 250ns to 1s |
| **Unique Capability** | 8-bit, 1 gigasample/s measure rate, good for advanced CMOS Pulse IV testing and high speed single pulse charge trapping | Dual-channel, quiescent point pulsing for scaled-down RF transistors | One multilevel pulse channel per DUT pin, integrated High Endurance Output Relay supports endurance testing of NAND and NOR |

[1] Full Width Half Maximum (FWHM)

# KTEI 6.2
**4205-PG2, 4200-SCP2, 4200-SCP2HR, 4200-PIV-A, 4200-PIV-Q, 4200-FLASH**

# Hardware/Software Upgrades and Pulse Applications Packages for the Model 4200-SCS

## 4205-PG2 Dual-Channel Pulse Generator Specifications[1]

The 4205-PG2 includes three operational modes for flexible, reconfigurable pulsing:

- Standard pulse
  - Pulse between any two voltage levels
  - Period range: 20ns to 1s
- Arbitrary (ARB) waveform
  - Output ARB waveforms built from standard wave libraries or sampled data
  - Depth: 256K points/channel
  - Timebase: 20ns/point up to 1sec/point, fixed timebase for entire waveform
  - Waveform Libraries: sine, ramp, square, triangle, gaussian, white noise
  - Input in .csv format
- Segment ARB™ waveform
  - With a single pulse channel, build multi-level and multi-pulse waveforms with user-defined line segments
  - Depth: 1024 segments/channel
  - Parameters for each segment: Segment #, start voltage, stop voltage, segment time, trigger out, High Endurance Output Relay (HEOR/SSR) on/off
  - Time per segment: 20ns to 1s, 10ns increments (each segment can have a different duration)

### PULSE/LEVEL[3]

| | | High Speed | High Voltage |
|---|---|---|---|
| $V_{OUT}$ | 50 Ω into 50 Ω | –5V to +5V | –20V to +20V |
| $V_{OUT}$ | 50 Ω into 1 MΩ | –10V to +10V | –40V to +40V |
| **Accuracy** | | ±(3% + 50 mV) | ±(3% + 100 mV) |
| **Amplitude/Level** | 50 Ω into 50 Ω | 1 mV | 5 mV |
| **Resolution** | 50 Ω into 1 MΩ | 2 mV | 10 mV |
| **Output Connectors** | | SMA | SMA |
| **Source Impedance** | | 50Ω Nominal | 50Ω Nominal |
| | | 1% | 1% |
| **Short Circuit Current** | | ±200 mA | ±800 mA |
| **Current into 50Ω Load (at full scale)** | | ±100 mA typical | ±400 mA typical |
| **Baseline Noise** | | ±(0.1% + 5 mV) RMS typical | ±(0.1% + 5 mV) RMS typical |
| **Overshoot/Pre-shoot/Ringing** | | ±5% of amplitude ±20mV | ±5% of amplitude ±80mV |
| **Output Limit** | | Programmable limit to protect the DUT | |

### TIMING

| | | High Speed | High Voltage |
|---|---|---|---|
| **Frequency Range** | | 1 Hz to 50 MHz | 1 Hz to 2 MHz |
| **Timing Resolution** | | 10 ns | 10 ns |
| **RMS Jitter (period, width)** | | 0.01 % + 200 ps typical | |
| **Period Range** | | 20 ns to 1 s (see Figure 1) | 500 ns to 1 s |
| **Accuracy** | | ±1% | ±1% |
| **Pulse Width Range** | | 10ns to (period – 10ns) | 250ns to (period – 100ns) |
| **Accuracy** | | ±(3% + 200 ps) | ±(3% + 5ns) |
| **Programmable Transition Time (0–100%)** | | 10 ns–1 s | 100 ns–1 s |
| **Transition Slew Rate[4]** | **Accuracy** | ±1% for transition time <100 ns | ±1% for transition time <1 µs |
| | **Linearity** | 3% for transition time <100 ns | 3% for transition time <500 ns |
| **Typical Minimum Transition Time 10–90%** | | <15 ns | <150 ns |
| | | Pulse period and width are variable in 10 ns steps without any output glitches or dropouts | |
| **Solid state relay** | **Open or close time** | 100 µs | |

### TRIGGER

**TRIGGER OUTPUT IMPEDANCE:** 50Ω.

**TRIGGER OUTPUT LEVEL:** TTL.

**TRIGGER IN IMPEDANCE:** 10kΩ.

**TRIGGER IN LEVEL:** TTL.

**TRIGGER IN TRANSITION, MAXIMUM:** <100ns.

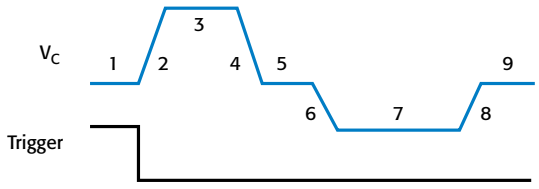
**TRIGGER IN TO PULSE OUT DELAY:** 560ns.

**TRIGGER SYNCHRONIZATION/JITTER[5]:** ±8ns.

1. Unless stated otherwise, all specifications assume a 50Ω termination.
2. Maximum number of PG2 cards depends on number and type of cards in the 4200 chassis.
3. Level specifications are valid after 50ns typical settling time (after slewing) for the high speed mode and after 500ns typical settling time (after slewing) for the high voltage mode into a 50Ω load
4. Specifications apply to a 10-90% transition, typical. Minimum slew rate for high speed range = 400mV/ms. For high voltage range = 2.00V/ms, which applies to both the standard pulse and Segment ARB™ mode
5. For multiple 4205-PG2 cards, when using appropriate cabling and the "trigger per waveform" trigger mode

All specifications apply at 23° ±5°C, within one year of calibration, RH between 5% and 60%, after 30 minutes of warmup.

| Segment | Start V | Stop V | Time | Trigger | HEOR/SSR |
|---|---|---|---|---|---|
| 1 | 0 | 0 | 10 µs | Y | Closed |
| 2 | 0 | 15 | 5 µs | N | Closed |
| 3 | 15 | 15 | 15 µs | N | Closed |
| 4 | 15 | 0 | 5 µs | N | Closed |
| 5 | 0 | 0 | 10 µs | N | Closed |
| 6 | 0 | –10 | 5 µs | N | Closed |
| 7 | –10 | –10 | 25 µs | N | Closed |
| 8 | –10 | 0 | 5 µs | N | Closed |
| 9 | 0 | 0 | 10 µs | N | Closed |




**Example of Segment ARB™ setup table and resultant waveform and trigger output**

# KTEI 6.2
**4205-PG2, 4200-SCP2, 4200-SCP2HR, 4200-PIV-A, 4200-PIV-Q, 4200-FLASH**

# Hardware/Software Upgrades and Pulse Applications Packages for the Model 4200-SCS

## 4200-SCP2 1.25GS Dual-Channel Oscilloscope Card and 4200-SCP2HR 200MS Dual-Channel Oscilloscope Card Specifications[1]

### ANALOG INPUT[1]

| | 4200-SCP2 | 4200-SCP2HR |
|---|---|---|
| **No. of Channels** | 2 | 2 |
| **Bandwidth (50Ω)** | DC to 750 MHz | DC to 250 MHz, typical |
| **Bandwidth (1MΩ)** | DC to 350 MHz | DC to 125 MHz, typical |
| **Full Scale Input Range (50 Ω)** | 0.05, 0.1, 0.25, 0.5, 1, 2, 5, 10 (Vp-p) | 0.05, 0.1, 0.25, 0.5, 1, 2, 5, 10 (Vp-p) |
| **Full Scale Input Range (1 MΩ)** | 0.1, 0.2, 0.5, 1, 2.5, 5, 10, 20, 50, 100 (Vp-p) | 0.25, 0.5, 1.25, 2.5, 5, 10, 25, 50 (Vp-p) |
| **DC Gain Accuracy** | <±1% of full scale | < ±0.25% of full scale |
| **Impedance** | 1 MΩ\|\|12 pF or 50 Ω | 1 MΩ\|\|12 pF or 50 Ω |
| **Impedance Accuracy** | ±1% | ±1% |
| **Coupling** | DC or AC | DC or AC |
| **Offset Adjust** | ±(full scale range/2) | ±(full scale range/2) |
| **Offset Accuracy** | ±(1% offset + 1% full scale) | ±1% |
| **Input Connectors** | BNC | BNC |
| **Absolute Maximum Input (50 Ω)** | ±5V DC | ±5V DC |
| **Absolute Maximum Input (1 MΩ)** | ±210V DC | ±210V DC |

### ANALOG-TO-DIGITAL CONVERTER

| | 4200-SCP2 | 4200-SCP2HR |
|---|---|---|
| **Resolution** | 8 bit | 16 bit |
| **Sample Rate** | 2.5 kS/s to 1.25 GS/s in 1, 2.5, 5 steps | 10 kS/s to 200 MS/s in 1, 2.5, 4, 5 steps |
| | 2.5 GS/s (1 channel interleaved) | 400 MS (1 channel interleaved) |
| **Memory Depth** | 1 MS/channel<br>2 MS on 1 channel, interleaved | 1 MS/channel<br>2 MS on 1 channel, interleaved |
| **Acquisition Time Range** | 50 ns to 419 seconds | 250 ns to 3,355 seconds |
| **Acquisition Modes** | Normal, Average, Envelope, and Equivalent-time | Normal, Average, Envelope, and Equivalent-time |

### TRIGGER

| | 4200-SCP2 | 4200-SCP2HR |
|---|---|---|
| **Trigger Source** | Channels 1 or 2, External, Pattern, Software | Channels 1 or 2, External, Pattern, Software |
| **Post-Trigger Delay** | 0 to 655 seconds | 0 to 655 seconds |
| **Pre-Trigger Delay** | 0 to waveform time | 0 to waveform time |
| **Trigger Hold Off Range** | 0 to 655 seconds | 0 to 655 seconds |
| **Trigger Modes** | Edge or Pulse Width | Edge or Pulse Width |
| **Edge Trigger Mode** | Rising or Falling Edge | Rising or Falling Edge |
| **Pulse Width Range** | 20ns to 655 seconds, 10ns resolution | 20ns to 655 seconds, 10ns resolution |
| **External Trigger Input** | TTL Compatible, 10 kΩ input impedance | TTL Compatible, 10 kΩ input impedance |
| **Connector** | SMB | SMB |

### OPTIONAL SCOPE PROBE: 4200-SCP2-ACC

**BANDWIDTH:** 70 MHz (4200-SCP2); 15MHz (4200-SCP2HR)

**ATTENUATION:** 1×

**MAX DC:** 300V DC rated.

**LOADING:** 100pF and 1MΩ.

**LENGTH:** 1m.

**CONNECTOR:** BNC.

### NOTES

1. Inputs are referenced to 4200 chassis ground

All specifications apply at 23°±5°C, within 1 year of calibration, RH between 5% and 60%, after 30 minutes of warmup.

# KTEI 6.2

**4205-PG2, 4200-SCP2, 4200-SCP2HR, 4200-PIV-A, 4200-PIV-Q, 4200-FLASH**

# Hardware/Software Upgrades and Pulse Applications Packages for the Model 4200-SCS

## 4200-PIV-A Pulse I-V Option

The 4200-PIV-A package combines the 4205-PG2 dual-channel pulse generator with the 4200-SCP2 oscilloscope, a specialized interconnect, and patent-pending software to provide a turnkey pulse I-V solution. The software controls sourcing from the pulse generator and data acquisition from the digital oscilloscope to automate a variety of pulse I-V tests. The Model 4200-SCS's proven interface handles instrument setup and control, as well as data storage and presentation. The innovative software provides both patented cable compensation and patented load-line compensation, producing DC-like I-V transistor curves, such as $V_{DS}$–$I_D$ family of curves and $V_{GS}$–$I_D$ for voltage threshold extraction. This solution provides pulse I-V testing to address charge trapping problems for high κ gate structures, and to eliminate self-heating issues in devices such as high power transistors and advanced CMOS on SOI technology. The specialized interconnect solves most of the problems typically encountered in high speed pulse testing:

- Combining pulse and DC sources to a single DUT pin permits both DC and pulse characterization without the need for re-cabling or switching
- Impedance matching, which minimizes reflection and maintains pulse fidelity
- Easy setup as a result of straightforward cabling and connection to the DUT

The pulse I-V package provides an easy-to-understand solution right out of the box, and offers access to the pulse generator and scope for general purpose pulse and scope applications.

Pulse I-V for leading-edge CMOS devices:

- Pulse voltage on gate, DC bias on drain
- Measure drain current and gate pulse voltage
- ±5V pulses for the gate (40ns to 150ns), ±200V DC for the drain

Included tests:

- $V_{DS}$–$I_D$: Both pulse and DC.
- $V_{GS}$–$I_D$: Both pulse and DC.
- Single-pulse scope view: Useful for setup validation, pulse width optimization, and prototyping of novel pulse tests.

## 4200 Pulse I-V for CMOS Typical Specifications[1]

**CHANNELS:** 2.

**TYPICAL PULSE PERFORMANCE (with 4205 Remote Bias Tee[4], Figure 2):**

- **Measurement Accuracy:** <4% of signal ±1mV.
- **Maximum Current Measure:** 100mA.
- **Resolution:** 100nA[2].
- **Offset:** <500nA.
- **Sample Rate:** 1GS/s.
- **Duty Cycle:** <0.1%.
- **DC Offset:** ±200V.
- **Minimum Transition Time (10–90%):** <15ns.
- **Pulse Source Voltage Range:** 0 to ±5V into gate.
- **Pulse Width:** 40ns to 150ns.

**SMU TYPICAL DC PERFORMANCE (with 4205 Remote Bias Tee):**

- **Leakage:** 1–10nA/V[3].
- **Noise:** 1–10nA RMS.
- **Maximum Voltage:** 210V (>40V requires safety interlock and related precautions).
- **Maximum Current:** 0.5A.

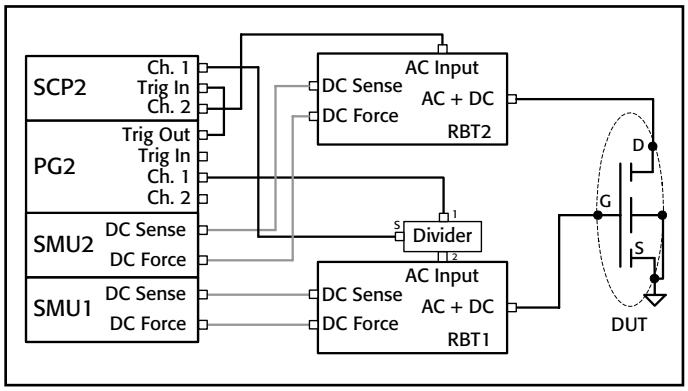
**4205 REMOTE BIAS TEE TYPICAL PERFORMANCE:**

- **Band Pass:** 3.5kHz–300MHz (3dB).
- **Power Divider Max Power Input:** 0.125W DC.

**NOTES**

1. Unless stated otherwise, all specifications assume a 50Ω termination.
2. When using Adaptive filtering.
3. Leakage measured after a 5 second settling time.
4. All typical specs apply to the AC+DC output connector of the 4205 Remote Bias Tee and after system compensation.

All specifications apply at 23°±5°C, within one year of calibration, RH between 5% and 60%, after 30 minutes of warmup.




**Interconnection for 4200-PIV-A for leading edge CMOS, high K and isothermal testing. PIV-A pulses the voltage on the gate and provides a DC bias on the drain.**

# KTEI 6.2

**4205-PG2, 4200-SCP2, 4200-SCP2HR, 4200-PIV-A, 4200-PIV-Q, 4200-FLASH**

# Hardware/Software Upgrades and Pulse Applications Packages for the Model 4200-SCS

## 4200-PIV-Q Pulse I-V with Q point and Dual Channel Pulsing

The 4200-PIV-Q package is designed for quiescent point pulsing for scaled-down RF transistors, such as HEMT and FET devices in III-V or LDMOS technologies. This package supports a number of new pulse testing capabilities by combining multiple 4205-PG2s and the 4200-SCP2HR oscilloscope. These new capabilities include dual-channel pulsing (i.e., for pulsing on both the gate and the drain simultaneously), higher power pulsing than the 4200-PIV-A package, and pulsing from a non-zero quiescent point. Pulse widths can be adjusted from 500ns to near-DC, and the same setup can also be used for performing true DC tests without re-cabling the system. The software controls sourcing from the pulse generators and data acquisition with the digital oscilloscope to automate a variety of pulse I-V tests. The Model 4200-SCS's proven interface handles instrument setup and control, as well as data storage and presentation. The innovative software provides both patented cable compensation and patented load-line compensation, producing DC-like I-V transistor curves, such as a $V_{DS}$–$I_D$ family of curves and $V_{GS}$–$I_D$ for voltage threshold extraction. The PIV-Q package will be useful for a variety of large signal tests on high frequency transistors, as well as for investigation of dispersion phenomena and device performance at speed. It also offers a good approach for avoiding the isothermal problems inherent in DC testing,

The PIV-Q package provides an easy-to-understand solution right out of the box, while offering access to the pulse generators and scope for general purpose pulse and scope applications.

Dual-channel pulse I-V testing for III-V and LDMOS:

- Pulse voltage on Gate and Drain.
- Measure: gate current, drain voltage and current.
- ±20V pulses for the gate, ±38V pulses for the drain.
- Pulse Widths: 500ns to 999ms.

Included tests:

- $V_{DS}$–$I_D$: Both pulse and DC.
- $V_{GS}$–$I_D$: Both pulse and DC.
- Single-pulse scope view: Useful for setup validation, pulse width optimization, prototyping of novel pulse tests.

## 4200-PIV-Q Typical Specifications[1]

**CHANNELS:** 2.

**TYPICAL PULSE PERFORMANCE:**

**Measurement Characteristics:** Gate Current: <50μA offset, 10μA resolution [2,4].
Drain Current: <50μA offset, 10μA resolution [2,4].

**Maximum Current Measure:** Gate: 100mA (into 50Ω).
Drain: 800mA (into 50Ω).

**Sample Rate:** 200MS/s.

**Duty Cycle:** 0.005% to 99.9%.

**Minimum Transition Time (10–90%):** 150ns.

**Gate/Base Pulse Source:** –20V to +20V.

**Drain/Collector Voltage Range:** –38V to +38V.

**Pulse Width:** 500ns to 999 ms.

**SMU TYPICAL DC PERFORMANCE:**

**Typical DC Leakage, Gate:** <20nA offset for <35V.

**Typical DC Leakage, Drain:** <10nA/V[3] for <35V.

**Typical DC Noise, Gate:** < 20nA RMS.

**Gate Offset:** <20nA.

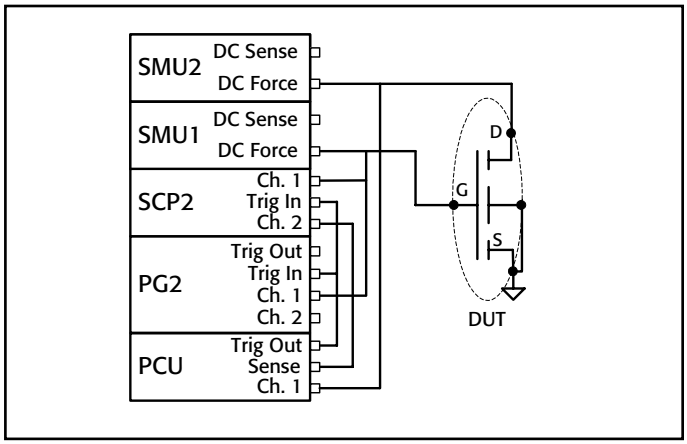
**Typical DC Noise, Drain:** <300pA RMS.

**Maximum Voltage:** 210V (> 40V requires safety interlock and related precautions).

**Maximum Current:** 1A[5].

**NOTES**

1. Unless stated otherwise, all specifications assume a 50Ω termination.
2. Offset and resolution specified when using Adaptive Filtering.
3. Leakage measured after a 5 second settling time.
4. All typical specs apply to the AC+DC output cable (from the SMU Force, connected to the SMA tee attached to Triax to SMA adapter).
5. For the high power 4210-SMU. For the medium power 4200-SMU, the maximum current is 100 mA. All specifications apply at 23°±°5C, within 1 year of calibration, RH between 5% and 60%, after 30 minutes of warmup.




**Interconnection for 4200-Q for III-V and LDMOS scaled-down RF transistors. PIV-A pulses voltage on both the gate and drain from non-zero bias (quiescent) conditions.**

# KTEI 6.2

**4205-PG2, 4200-SCP2, 4200-SCP2HR, 4200-PIV-A, 4200-PIV-Q, 4200-FLASH**

# Hardware/Software Upgrades and Pulse Applications Packages for the Model 4200-SCS

## 4200-FLASH Non-volatile Memory Test Option

The 4200-FLASH package will test floating gate FLASH memory cells or small arrays quickly and easily. This package takes advantage of many of the new features added to the 4205-PG2 and includes all the necessary code and the interconnect needed to perform a standard set of Flash memory tests for NAND or NOR technologies, with higher pulse voltages important for MLC technologies. The tests included generate program and/or erase cycles using an easy interface to the patent-pending Segment ARB™ pulse mode as well as controlling the in-line High Endurance Output Relay. Endurance and Disturb tests are also a snap using the included test projects.

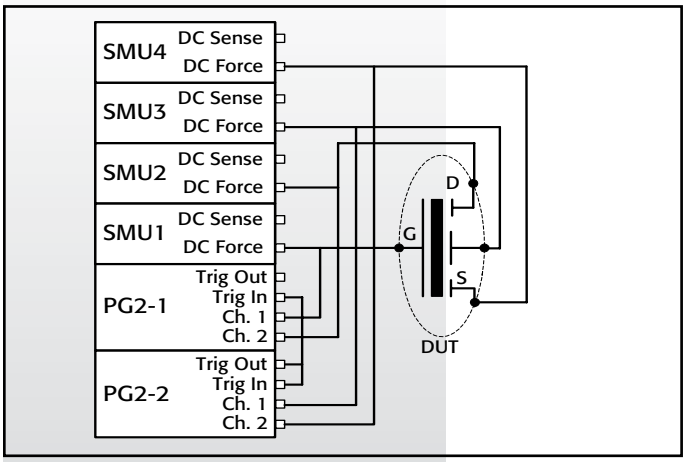
The FLASH package provides an easy-to-understand solution right out of the box, and offers easy access to the pulse generators for general purpose pulse applications.

Four channels of multi-level pulse:

- ±40V pulsing into high impedance pin (±20V into 50Ω).
- High Endurance Output Relay provides fast open/close for pin isolation during erase pulse.
- Pulse Widths: 250ns to 1s.
- Up to 25 pulse levels (100 pulse segments).

Included tests:

- Endurance.
- Program-read.
- Erase-read.
- Disturb.




Interconnect for 4200-FLASH for single DUT, shown with 4 SMUs and no external switch matrix. FLASH provides pulsing for program, erase and P+E stress waveforms and DC for Vt measurements.

## 4200-FLASH Typical Specifications[1]

**CHANNELS:** 4 channels (optional 8 channels max).

**TYPICAL PULSE PERFORMANCE:**

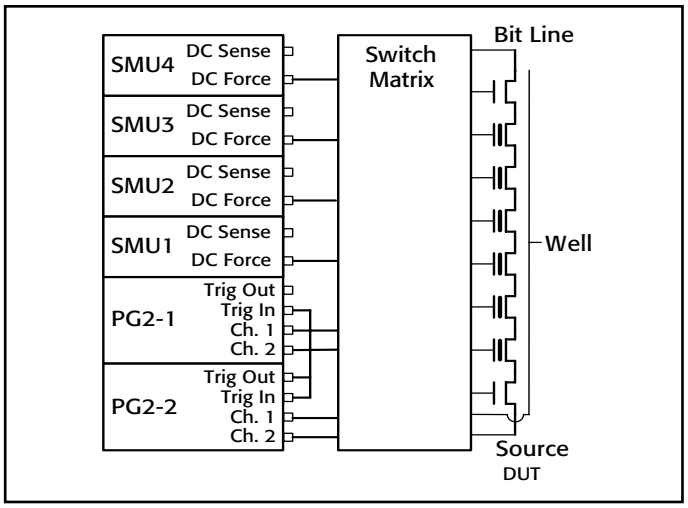
- **Number of voltage levels/waveform:** 25.
- **Minimum Transition Time:** 150ns.
- **Pulse Source Voltage Range:** 0 to ±20V into 50Ω. 0 to ±40V into high impedance.
- **Pulse Width:** 250ns to 1s.
- **Trigger Synchronization/Jitter:** ±8ns.
- **Switching time for DUT pin isolation:** 100μs.
- **HEOR Off Capacitance:** 250pF.

**SMU TYPICAL DC PERFORMANCE**

- **Typical DC Leakage:** <10nA/V[2] for <35V.
- **Typical DC Noise:** <300pA RMS.
- **Maximum Voltage:** 200V (>40V requires safety interlock and related precautions).
- **Maximum Current:** 1A[3].

**NOTES**

1 Unless stated otherwise, all specifications assume a 50Ω termination.
2 Leakage measured after a 5 second settling time.
3 For the high power 4210-SMU up to 20V. For the medium power 4200-SMU, the maximum current is 100 mA.




Interconnect for 4200-FLASH for addressable device, shown with 4 SMUs and external switch matrix. FLASH provides pulsing for program, erase and P+E stress waveforms and DC for Vt measurements.

# KTEI 6.2

**4205-PG2, 4200-SCP2, 4200-SCP2HR, 4200-PIV-A, 4200-PIV-Q, 4200-FLASH**

# Hardware/Software Upgrades and Pulse Applications Packages for the Model 4200-SCS



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