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WHITE PAPER

Introducing Pulsing into Reliability Tests for Advanced CMOS Technologies

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AC, or pulsed, stress is a useful addition to the typical stress-measure tests for investigating both semiconductor charge trapping and degradation behaviors. NBTI (negative bias temperature instability) and TDDB (time dependent dielectric breakdown) tests consist of stress/measure cycles. The applied stress voltage is typically a DC signal, which was used because it maps more easily to device models. However, incorporating pulsed stress testing provides additional data that permits a better understanding of device performance in frequency-dependent circuits.

Traditionally, DC stress and measure techniques have been widely used for characterizing the reliability of CMOS transistors, such as the degradation due to channel hot carrier injection (HCI) and Time Dependent Dielectric Breakdown (TDDB). However, the nature of reliability testing has evolved recently as new dynamic phenomena, such as Negative Bias Temperature Instability (NBTI) for Positive Metal-Oxide Semiconductor Field-Effect Transistors (PMOSFETs) and charge trapping in high κ gate stacks, emerge. These phenomena can have a major impact on evaluating the reliability of new processes. Additionally, there's growing interest in evaluating the reliability of circuits in actual operation, in which multiple devices are turned on and off dynamically.

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The use of new materials and structures has led to greater attention to dynamic reliability testing, introducing pulsed or AC stress into the reliability testing mix, as well as pulse during measurement to characterize interface degradation caused by applied stress.

It has been found that interface degradation, or an increase in interface trap density, caused by voltage stress over time, is a key contributor to device reliability issues such as HCI, NBTI, as well as reliability of high κ gate stacks [1]. Using charge pumping techniques to add interface trap monitoring tests to the existing DC characterization tests can be very useful in understanding these new reliability issues. In this white paper, we will discuss some charge pumping and AC stress techniques commonly used in reliability testing for advanced CMOS technologies.

Although the term "AC stress" is used frequently, it's a bit of a misnomer. For the applications discussed here, AC stress is actually a train of square or trapezoidal voltage pulses. For the purposes of this paper, we'll use the term "pulsed stress" because it doesn't imply a continuously time-varying, or alternating, signal.

Pulse Characterization - Charge Pumping

Charge pumping (CP) and simultaneous C-V (the combination of high frequency and quasistatic C-V) measurements are the two most common methods used to characterize the interface trap state densities in MOS devices. However, as transistor sizes are scaled down and gate oxides are made thinner, quasistatic C-V becomes impractical for oxide thicknesses of less than 3-4nm; therefore, that makes simultaneous C-V unsuitable for interface traps characterization on the new high κ materials [2].

CP is a useful technique for understanding gate stack behavior, which is increasingly important as high κ films become more commonly used for transistor gates. CP characterizes interface and charge-trapping phenomena. The change in the CP results can be used to determine the amount of degradation caused by typical reliability test methods, employing either DC or pulsed stress: hot carrier injection (HCI), negative bias temperature instability (NBTI), and time dependent dielectric breakdown (TDDB).

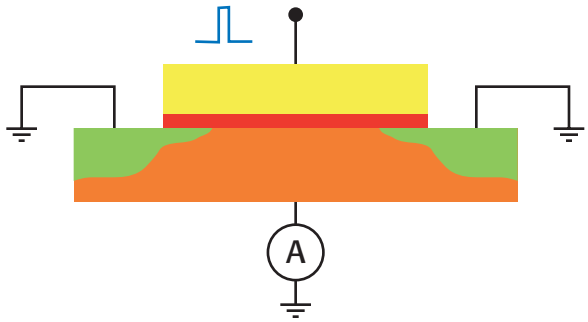

Figure 1. Schematic for charge pumping measurement. Source and drain of the transistor are connected to ground, while the gate is pulsed with fixed frequency and amplitude

Figure 1 shows the connections to the device under test (DUT). The basic CP technique consists of measuring the substrate current while applying voltage pulse trains of fixed amplitude, rise time, fall time, and frequency to the gate of the transistor. During this test, the drain, source, and body are tied to ground, with the body connected to ground with a Source-Measure Unit (SMU), which is used to measure the current through the gate (I_{CP}).

The two most common CP techniques are the base level sweep and the amplitude sweep. In a voltage base level sweep, the period (pulse width) and voltage amplitude are fixed, while the pulse base voltage is swept (***Figure 2a***). At each base voltage, the body current is measured and plotted against the base voltage (I_{CP} vs. V_{base}), as shown in the graph in ***Figure 2a***.

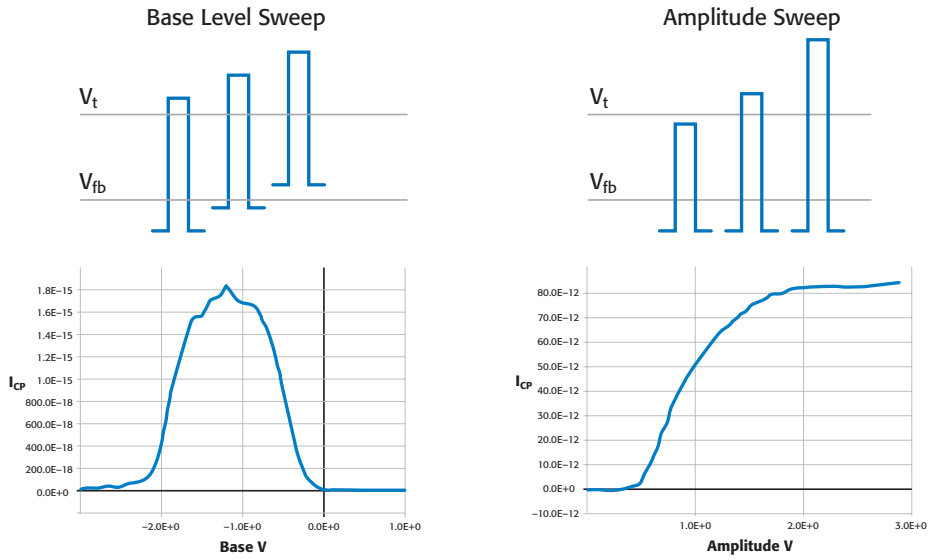

Figure 2a *Figure 2b*

Figure 2. Various pulse shapes and pulse sweeps for charge pumping: a) base voltage sweep, b) pulse amplitude sweep.

The second charge pumping technique is the voltage amplitude sweep, which has a fixed base voltage and period (pulse frequency) with voltage amplitude changed for each sweep step (***Figure 2b***). The data obtained is similar to that extracted from the voltage base sweep, but in this case, the charge pumping current is plotted against the voltage amplitude (I_{CP} vs. V). These measurements can also be performed at multiple frequencies (periods) to obtain the frequency response of the interface traps.

For high κ gate stack structures, the CP technique can quantify the trapped charge (N_{it}) as:

$$N_{it} = \frac{I_{CP}}{qfA}$$

That's possible because trapped charge beyond the silicon substrate/interfacial layer can be sensed [3]. The plot in ***Figure 2a*** shows the characteristic I_{CP} curve for the base voltage sweep, while the plot in ***Figure 2b*** shows the I_{CP} curve for the variable amplitude sweep.

The CP technique can also be used to characterize the initial stages of interface trap formation. ***Figure 3*** shows a CP measurement of a "fresh" (i.e., not previously tested) MOSFET, using a 1MHz frequency. The dark curve is the initial CP measurement; the lighter curves indicate subsequent measurements. Note that the shape of the I_{CP} curve changes, as well as the magnitude, at the lower voltages. After repeating the measurements a number of times, the change effectively stops as the effect saturates. The change in the curve shape indicates formation of interface traps due to electrical stress imposed by the CP measurement. This means that the CP measurement using pulses is effectively stressing the device and causing some degradation. The degradation under pulsed stress is a useful addition to our understanding of Bias Temperature Instability (BTI) and TDDB.

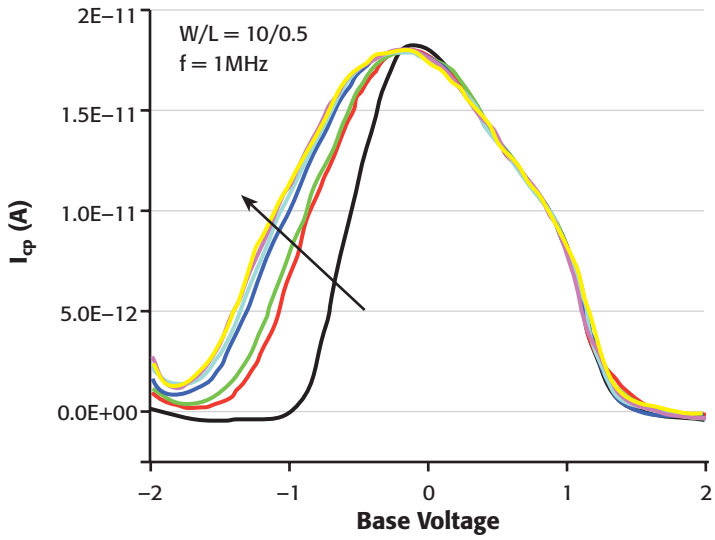

Figure 3. "Stress" effect induced by charge pumping measurement on a "fresh" device.

Pulsed Stress for BTI and TDDB

BTI (which includes both NBTI and PBTI) and TDDB share a similar test method. This method consists of two intervals, stress and measure, in which an elevated voltage is applied to stress the structure, alternating with a measurement that's performed periodically to determine the amount of degradation. Both NBTI and TDDB are performed with the device at an elevated temperature to accelerate degradation to reduce test times, which can range from an hour to two weeks.

Recently, NBTI was reported as an increasingly important reliability issue for PMOSFET. NBTI is a phenomenon where change in the gate-channel interface causes degradation in pMOS device performance [4]. The degradation is typically tracked as the increase of the transistor threshold voltage (V_T) and degradation of the drain current (I_D). This degradation can reduce yield through failures during burn-in or in the field [5, 6]. NBTI testing has a recently released industry standard [7]. The biggest test methodology difference between NBTI and traditional HCI testing is that there is a relaxation of stress-induced degradation when stress is removed during NBTI testing.

This relaxation presents a challenge to the traditional stress and measure technique, because there is always a transition period between the stress interval and the measure interval when no voltage is applied to the device, and relaxation occurs. Given that the instrumentation "sees" the device during measurement interval, after some relaxation has occurred, this technique will overestimate device lifetime because less degradation effect will

appear during the measurement phase. Also, using DC stress voltages may not accurately represent the stresses experienced by the device in a real-life circuit, because most devices will experience relaxation when transistor is not active; therefore, the DC stress technique may "underestimate" the transistor lifetime in a real circuit. With the shrinking reliability margins for new technology nodes, underestimating the transistor lifetime may be an unaffordable luxury.

In addition to relaxation as a dynamic reliability behavior, charge trapping has been found in transistors with high κ gate stacks. This is because the process for depositing high κ material in a CMOS process is still immature and there are a large amount of trap centers left in the film as compared to the SiO_2 gate process. When the gate is turned on, charges can be transiently trapped in the gate, changing the performance of the transistor over time, as trapped charges shift the transistor's threshold voltage. It may take from tens of nanoseconds to milliseconds to trap charges into the gate stacks, depending on the quality of the gate and trapping conditions.

The distribution of charges inside a high κ gate may also affect the electric field distribution, thereby altering the reliability behavior of the high κ gate, in terms of both TDDB and BTI [8]. At the same time, a similar relaxation effect exists due to de-trapping of charges at lower gate voltages. The relaxation will lead to an inaccurate estimate of device lifetime because it is strongly time dependent, while the stress-measure transition time, and thus relaxation time, is usually not well controlled in a test environment.

The dynamic nature of new reliability phenomena requires pulse stress to simulate in-circuit device performance. Different circuits and circuit topologies operate at different frequencies, so frequency dependent lifetime extraction may be needed to model lifetime based on frequency. In those applications, pulsed stress has advantages over the DC stress technique. Pulsed stressing applies a dynamic signal to the device, which better approximates the normal behavior of frequency-dependent circuits. During pulse stress, the stress is interrupted, and the degradation is at least partially recovered, which restores the device lifetime. The stress creates interface traps that are partially annealed, or repaired, during the time the stress is off. Because of this recovery (or self-annealing) behavior, reliability engineers and scientists are using the pulsed stress technique to gain a better understanding of device lifetime as it applies to in-circuit or in-product conditions.

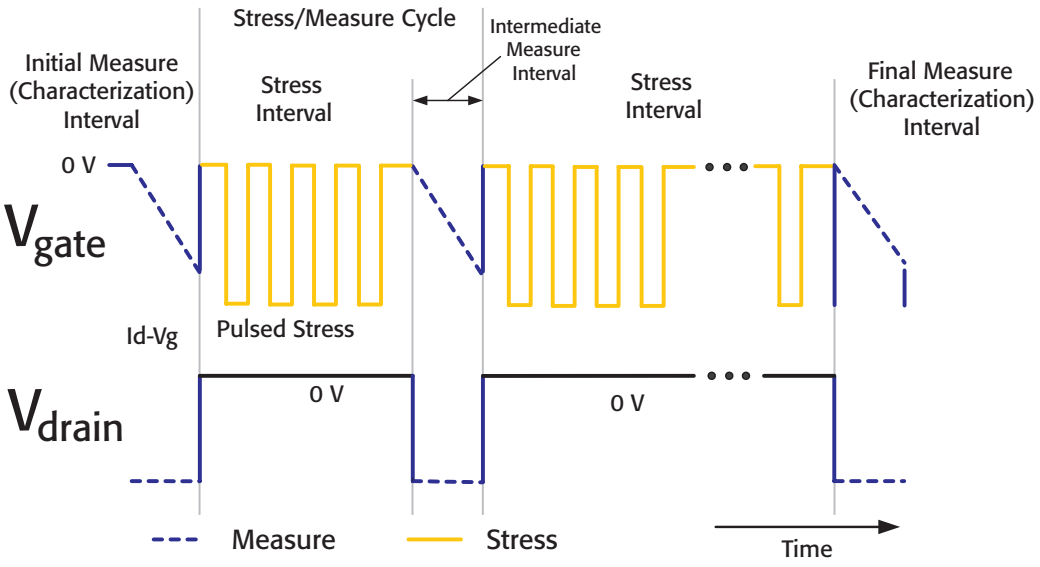

Figure 4a.

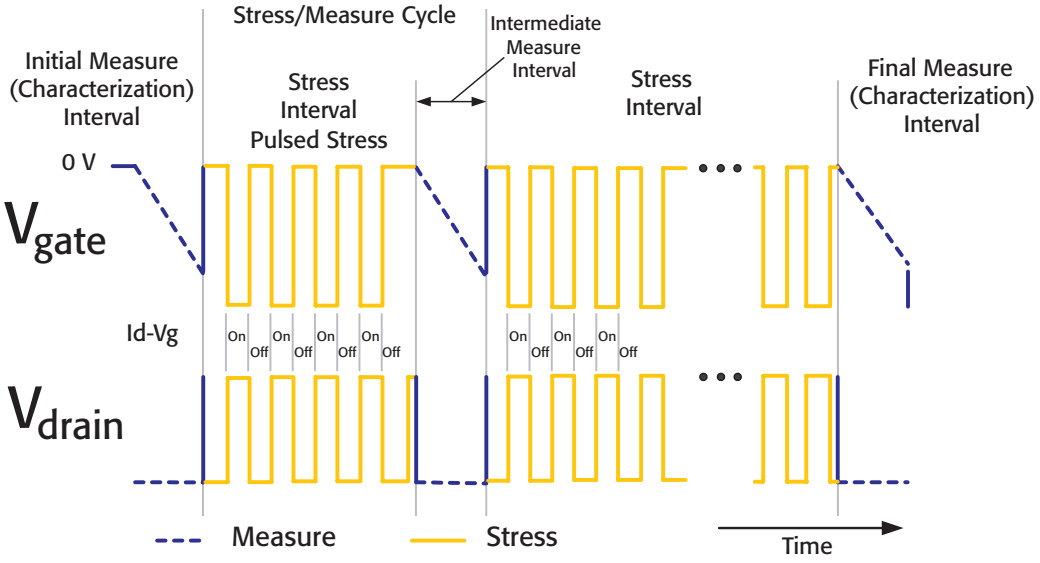

Figure 4b.

Figure 4. NBTI stress/measure diagram, showing two different pulsed stress methods: a) Dynamic NBTI (DNBTI), using traditional gate and drain voltages, b) DNBTI to simulate inverter conditions, with drain voltage in opposite phase to the gate voltage

By using a periodic stress that mimics the stress seen by the device in-circuit, the pulsed stress is basically a short DC stress interrupted by a time where no stress is applied (***Figure 4***). For NBTI, this off-stress portion between stress pulses permits the degradation to recover to some degree [9]. This partial recovery has significant implications in determining

and modeling the lifetime behavior of the device. The partial recovery is not yet well understood and may be different for each unique combination of device structure, dimensions, and materials used. ***Figure 4*** shows two examples of pulsed stress, although other pulsed stress methods are possible. ***Figure 4a*** shows pulsed stress for NBTI, where the drain voltage remains 0V during the stress interval. ***Figure 4b*** shows pulsed stress for NBTI, but where the drain voltage is pulsed, in addition to the gate voltage. This second method is used to simulate the performance of a single device in an inverter circuit. Both the gate and drain are being stressed in ***Figure 4b***, so there are both NBTI and HCI components in the device degradation. In general, the pulsed stress technique produces less degradation, permitting a longer device lifetime.

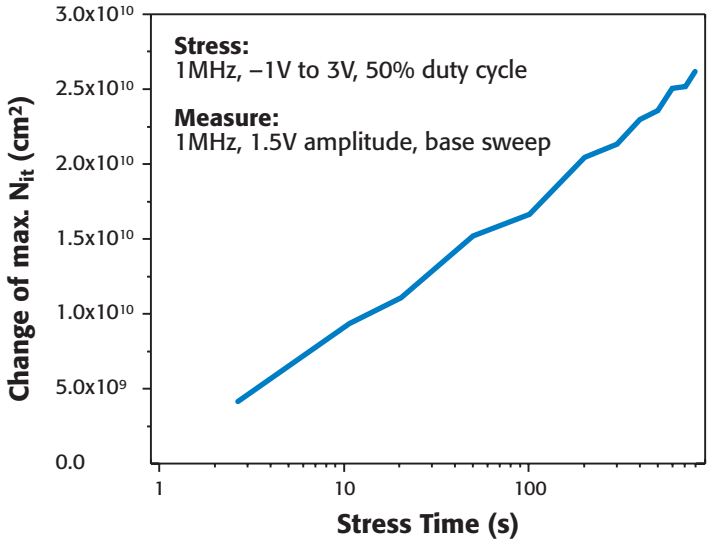

Figure 5. Degradation of N_{it} due to pulsed stress.

For NBTI, the pulsed stress technique is used to investigate dynamic behavior of individual devices [9], as well as digital circuits [10]. ***Figure 5*** shows the increase in Nit due to different durations of pulsed stress, combining the stress method shown in ***Figure 4a*** with the periodic CP measurements shown in ***Figure 2a***.

In addition to BTI, the role of TDDB must also be understood in both static and dynamic breakdown regimes [11, 12]. For monitoring SILC (stress-induced leakage current) during TDDB testing, the stress/measure diagram is similar to ***Figure 4a*** but the V_{drain} is kept at a constant non-zero voltage, permitting I_d to be read during stress.

Conclusion

Pulsed voltage provides a key capability for investigating inherent material, interface, and reliability properties of high κ films, and devices based on these new films. Pulsing a voltage while simultaneously measuring the DC current is the basis for charge pumping, which is valuable for measuring inherent charge trapping. Used in conjunction with DC or pulsed stress, CP can also study charge trapping, as well as new charge creation on the high κ-Si interface and within the high κ film. Pulsed stress also provides a stress method that better mimics actual stresses seen by the in-circuit devices, which is useful for various device reliability tests, including BTI, TDDB, and HCI. In addition, pulsed stress provides insight into device reliability behaviors not available using DC stress. Pulsed stress complements traditional DC techniques to provide a better understanding of device reliability behavior.

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