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WHITE PAPER

Pulsed Characterization of Charge-Trapping Behavior in High κ Gate Dielectrics

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High κ Material Research

High dielectric constant (high κ) gate materials, such as hafnium oxide (HfO_2), zirconium oxide (ZrO_2), alumina (Al_2O_3), and their silicates[1], have drawn a great deal of attention in recent years as potential materials for gate dielectrics in advanced CMOS processes. Due to their high dielectric constants, high κ gates can be made thicker than SiO_2 while achieving the same gate capacitance. The result is much lower leakage current – as many as several orders of magnitude lower.

While high κ material can help solve gate leakage problems with leading-edge processes, there still are some remaining challenges. Associated with this advantage are several technical hurdles such as V_t instability[2-4], carrier channel mobility degradation[5-8], and long-term device reliability[9-12]. One important factor attributed to those issues is trapping of charges in the pre-existing traps inside the high κ gate dielectrics[13-14]. When the transistor is turned on, some of the channel carriers will be accumulated in the gate dielectric due to the vertical electrical field, resulting in a shift of threshold voltage and a reduction in drain current.

Fully understanding the charge-trapping mechanism is the key to understanding the source of channel mobility degradation and device reliability issues associated with high κ gate dielectrics. This white paper discusses

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the nature of the charge trapping and the limitation of DC characterization techniques in quantifying trapped charge. Then, it describes an ultra-fast pulse I-V technique for characterizing the intrinsic ("trap free") performance of high κ gate transistors that exhibit the charge-trapping effect.

Charge-Trapping Phenomena

The effect of charge trapping is decreased drain current after the transistor is turned on. As charges are trapped in the gate dielectric, the threshold voltage of the transistor increases due to the built-in voltage in the gate capacitor; therefore, the drain current decreases. ***Figure 1*** illustrates charge trapping in the gate dielectric as the transistor is turned on.

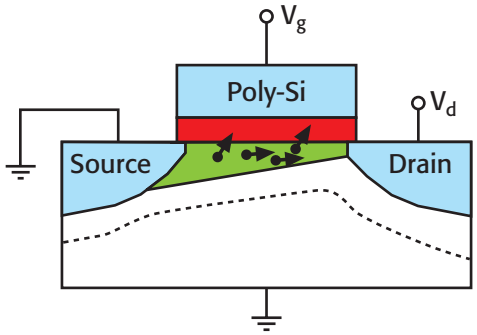


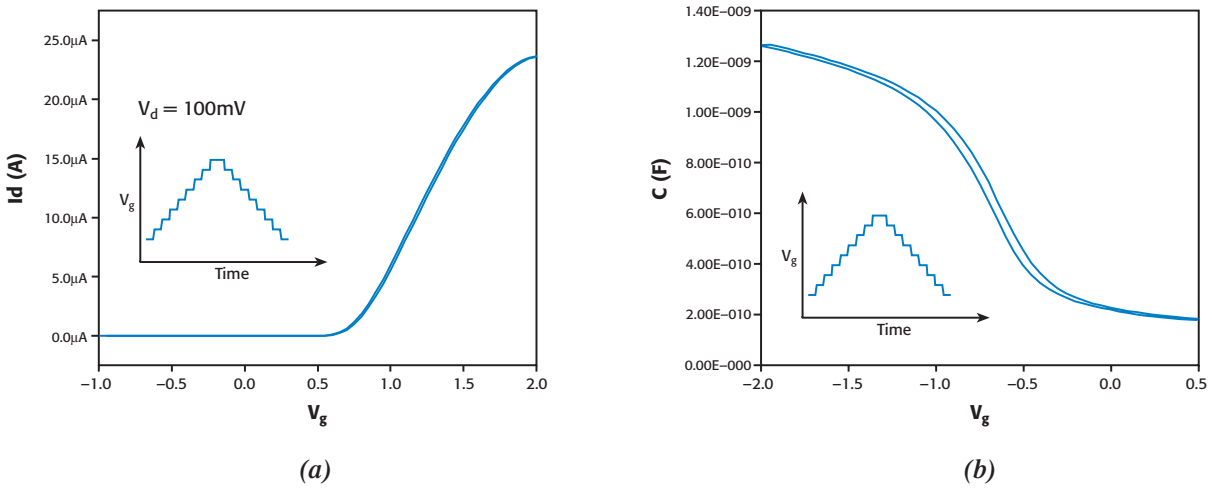
Figure 1. Charge trapping during transistor "turn-on."

It has been reported that charge trapping and de-trapping times strongly depend on the composition of gate stacks, i.e., physical thickness of the interfacial SiO_2 layer and high κ film, as well as process techniques[15-17]. The time scale varies from less than a microsecond to tens of milliseconds[18]. The de-trapping of the charges is also strongly gate voltage and polarity dependent. The wide dynamic range of charge trapping, and the voltage dependent trapping and de-trapping, make it very difficult to use one type of characterization technique, especially DC techniques, to get a complete picture of what is going on inside the stacked gate dielectric. A faster measurement technique is desirable to capture the dynamic nature of the charge-trapping behavior.

Limitation of DC Characterization Techniques

There are several ways of detecting charge-trapping phenomena. One easy and commonly used method is to use a double sweep in either DC V_{gs}-I_d or high frequency C-V measurements. These techniques involve ramping gate voltage back and forth while drain current or gate capacitance is measured. If hysteresis is seen on the resulting I-V or C-V

curves, it is a clear indication of charge trapping inside the gate stacks. ***Figure 2*** shows two examples of the hysteresis seen in V_{gs}-I_d or C-V curves from devices with a high κ dielectric.



(a) *(b)*

Figure 2. DC I-V and C-V curves showing hysteresis due to charge trapping by using a double sweep technique (backward and forward sweep).

The issue with this technique is that the hysteresis is strongly dependent on measurement time. The hysteresis measured in the DC I-V test is different from that in a C-V test, because the time taken for each measurement can be dramatically different. Another example to illustrate the shortcoming of this technique is shown in ***Figure 3***. In this experiment, dual sweep C-V measurements were taken at different speeds. One can clearly see the changing of the hysteresis as the test speed changed. In reality, the test speed is not easily controlled, as it is strongly dependent on instrumentation. Even if test speed is controlled, there is no model to quantify how much charge is really trapped in the gate during the test. So, while signs of hysteresis in the result are a good indication of charge trapping, it cannot quantify the amount of charge trapped, since most fast transient trapping will be lost in the DC measurement.

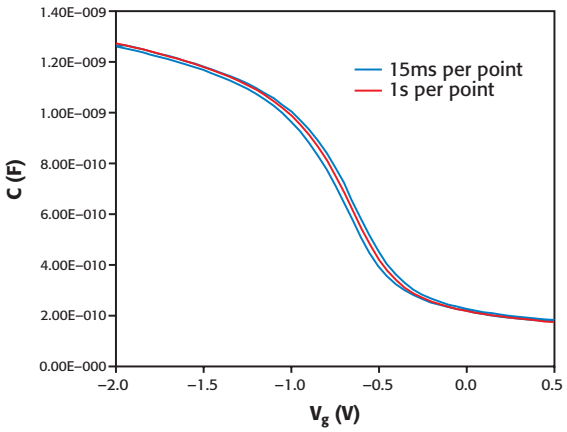


Figure 3. Time-dependent hysteresis of C-V: Slower measurements produce less hysteresis, indicating an equilibrium condition has been reached.

Another frequently cited method for quantifying trapped charges is to use DC stress to inject charges intentionally into the gate, then use the C-V or I-V method to measure the flat band voltage or threshold voltage shift[19]. The amount of charge trapped can be calculated based on this formula:

$$Q_{trap} = C_{gate} \cdot \Delta V_{fb}, \text{ or } Q_{trap} = C_{gate} \cdot \Delta V_{t}$$

The issue with this technique is that, between DC stress and I-V or C-V measurement, there is typically a transition period when there is no applied voltage, or the voltage is very low compared to the stress voltage condition. As mentioned earlier, when the stress voltage is off, the charges trapped in the gate can de-trap in as few as tens to hundreds of microseconds. So, only a fraction of the total trapped charges are measured due to relaxation during the transition between the stress and measure intervals. Underestimation of the charge trapping gives an incorrectly "optimistic" view of the quality of the film.

Recently, an "on-the-fly" method[20] was introduced for measuring the threshold voltage shift without relaxation for NBTI type measurements. However, in applying this technique to high κ gate stacks, it may not quantify all of the fast transient traps, because it is still a DC test.

Ultra-short Pulse Characterization Techniques

Better methods have been developed over the past few years[3,4,18,21] for capturing the fast transient behavior of charge trapping. ***Figure 4*** shows two different test configurations for a Single Pulse Charge Trapping (SPCT) measurement. In each measurement setup, a pulse is

applied to the gate of the transistor while its drain is biased at a certain voltage. The change in drain current, resulting from the gate pulse, appears on the digital oscilloscope.

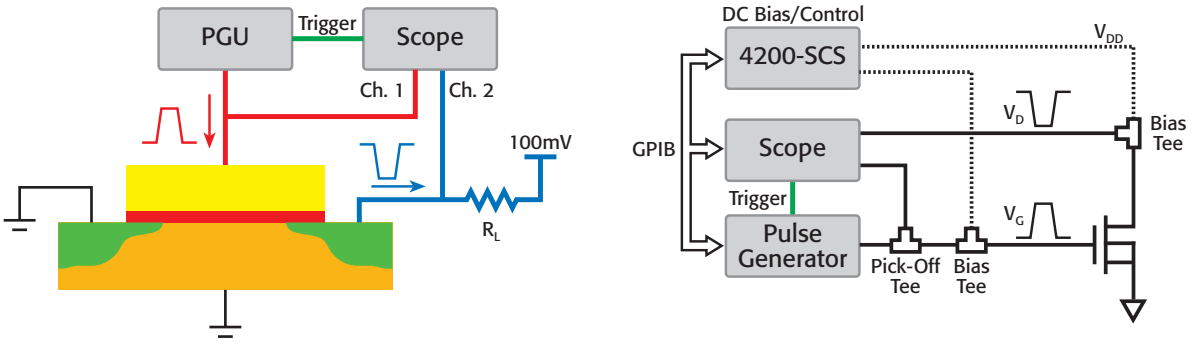


Figure 4. Two different pulse I-V test setups to study transient charge trapping inside high κ gate stack.

The difference between these two configurations is that the one in ***Figure 4b*** has much higher bandwidth than the one in ***Figure 4a***; therefore, it can capture much faster pulse responses (down to tens of nanoseconds). At such high speed, the bulk traps in a high κ layer are unlikely to respond; therefore, an "intrinsic" transistor response with negligible charge-trapping effect can be measured.

The key to using the single pulse method is to look at the charge trapping and de-trapping behavior within a single, well-configured gate pulse (***Figure 5***). The gate pulse usually starts in a position that discharges the gate capacitor before the voltage ramp begins. This is to clean up any residual charges that might be trapped in the gate. Then, during the rise time of the voltage ramp, the corresponding drain current response is captured, allowing a V_{gs}-I_d curve to be formed.

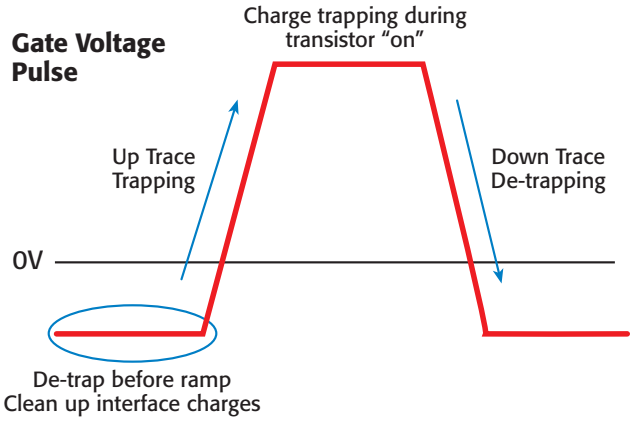


Figure 5. Trapping and de-trapping in single gate voltage pulse.

If the pulse rise time is fast enough so that there is no charge trapping, then the V_{gs}-I_d curve represents the intrinsic behavior of the transistor, free from the error due to the charge-trapping effects[15]. During the plateau of the pulse, the transistor is turned on, and some of the channel carriers might be trapped in the gate, which changes the threshold voltage and causes the drain current to drop. During the fall time of the pulse, another V_{gs}-I_d curve is formed, but with the charge-trapping effect.

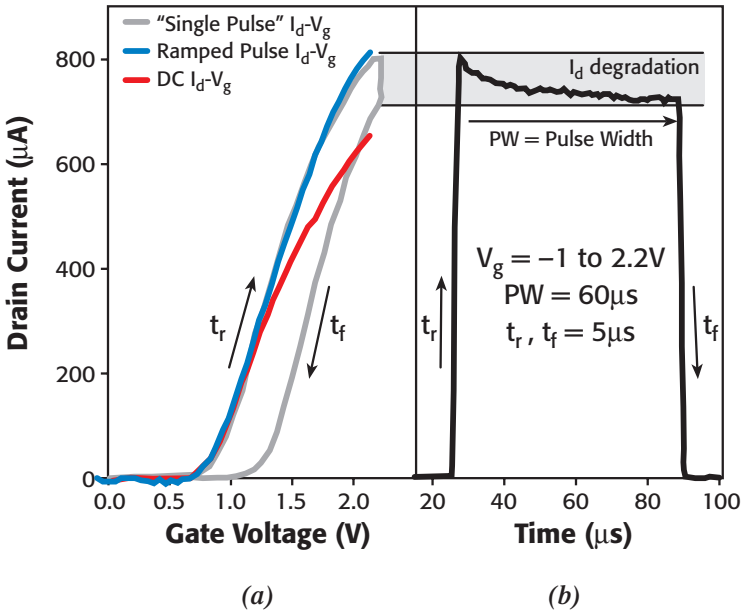


Figure 6. Single Pulse Charge Trapping measurements: a) the ultra-short ramped pulse I_d-V_g and slow "single pulse" pulse with hysteresis (DC result is shown as a reference), and b) corresponding slow pulse versus time illustrating an alternative approach to determine the degradation of I_d.

Figure 6 shows an example of a pulse I-V measurement with different pulse speeds using setups from ***Figures 4a*** and ***4b*** respectively. A DC I-V curve is overlaid for comparison. There is hysteresis with the slower pulse due to charge trapping. By using the faster pulse, hysteresis is eliminated because there's insufficient response time for charges to be trapped.

Even though the hysteresis of a pulse I-V curve from a slower pulse can quantify charge trapping much better than a DC method, results should be interpreted with caution. This is due to de-trapping effects being influenced by the specific structure of the gate stack under test and the pulse fall time. Also, when two traces in the t_r and t_f portions are not parallel, it is difficult to define the point at which hysteresis is measured. Therefore, slower pulse measurements should only be used for high κ devices with relatively low charge-trapping effects. An alternative approach is to plot the pulse I_d versus time (***Figure 6b***). Here,

an evaluation of the pulse width portion of I_d (where I_d degrades) can be used to quantify trapped charge[14,15].

When the charge-trapping effect is significant, the more legitimate method is to use a fast pulse with short rise and fall times. This measurement method produces I_d-V_g values by using a single pulse per point of less than 100ns. This can be easily achieved with the ultra-short pulse technique shown in ***Figure 4b***.

Benefits of Short Pulse Characterization

Since there is much less charge-trapping effect with very short pulse widths, the drain current measured is higher than under DC conditions (red curve, ***Figure 6***). This results in a higher predicted channel carrier mobility when pulse I-V data are used to generate a model, which is more representative of transistors that are switching very fast (i.e., those that will not experience full charge-trapping effects).

Another advantage of the ultra-short pulse system is that the pulse I-V measurements, with pulse widths on the order of nanoseconds, can be performed very easily and results can be compared to a DC measurement without resetting the system hardware or moving the wafer to another station. Such a comparison is shown in ***Figure 7***.

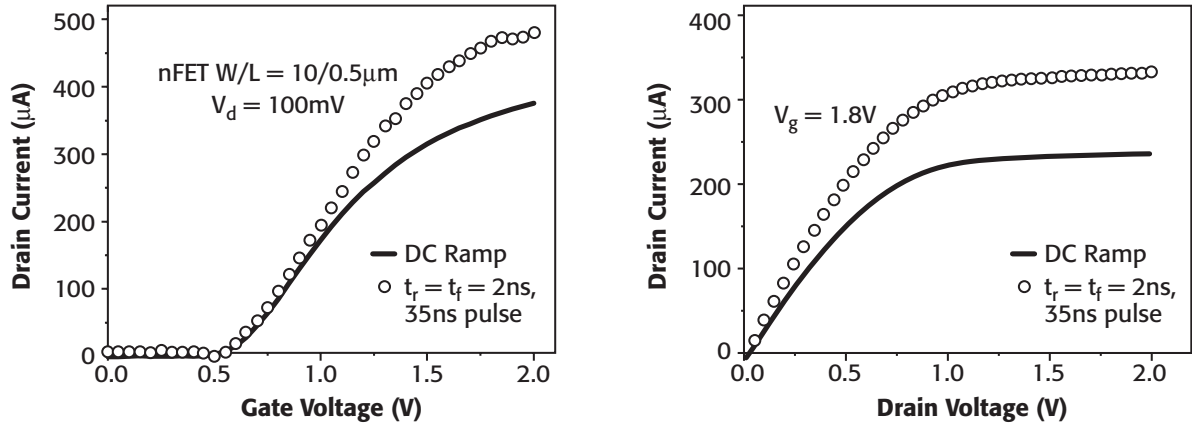


Figure 7. Overlay of pulse I-V and DC I-V measurements on NMOSFET with high κ gate dielectrics: (a) DC and pulsed I_d-V_g measurement at linear region, (b) DC and pulsed I_d-V_d measurement.

The data in ***Figure 7*** were collected by using ramped pulse I-V measurements on an HfO_2 gate transistor with 2ns rise and fall times, and a 35ns pulse width. For the V_{gs}-I_d test, gate pulses were ramped from 0 to 2.0V and, at each gate pulse, drain current response was

captured on the scope through a 50Ω sense resistor. For the V_{ds}-I_d test, the gate pulse was fixed while the drain voltage (biased by a SMU through the bias Tee) was ramped. At each drain bias point, the drain current in response to a gate pulse was captured by the scope. The pulse was set such that close-to-intrinsic drive current could be measured and compared to the DC measurement.

Drive current measured using the pulse I-V technique is significantly higher than DC due to the lack of charge-trapping effects. This illustrates the close-to-intrinsic performance of transistors with high κ gate dielectrics, and ultimately demonstrates the advantage of the ultra-short pulse I-V technique.

Because of the complications associated with trying to characterize charge-trapping effects for transistors with different functionalities, it would be nice if modeling engineers did not have to worry too much about it. CMOS devices are often used in high frequency operating conditions, so the real device performance is closer to that depicted by the ultra-short pulse measurement technique, rather than by a DC measurement[23]. Therefore, the best solution for modeling engineers is to use instrumentation and a test configuration that avoids artifacts associated with DC or slower pulse measurements. The resulting models will help optimize designs for the operating conditions.

Process engineers also need these pulse measurement techniques to characterize and track improvements in their continuing efforts to improve film quality and remove charge-trapping degradation. Finally, an understanding of the intrinsic behavior of high κ gate dielectric devices is key to understanding the physics of charge trapping and de-trapping. This physical-based understanding leads to the correct extrapolation of device lifetime.

Sources of Error

It's important to be very careful when using the ultra-short pulse technique. The speed characteristics of the ultra-short pulse are in the radio frequency (RF) domain, so it is very easy to introduce errors in the measurement if the test system is not optimized for high bandwidth. There are three main sources of errors: signal losses due to cables and connectors, losses due to device parasitics, and contact resistance.

Signal losses due to cables and connectors, as well as contact resistance effects, can be calibrated out using a transistor with an SiO_2 gate, where there is no charge-trapping effect. The pulse I-V curve should overlay the DC I-V curve precisely once the calibration is complete. ***Figure 8*** shows an example plot of DC and pulse I-V measurements on a MOSFET with an SiO_2 gate.

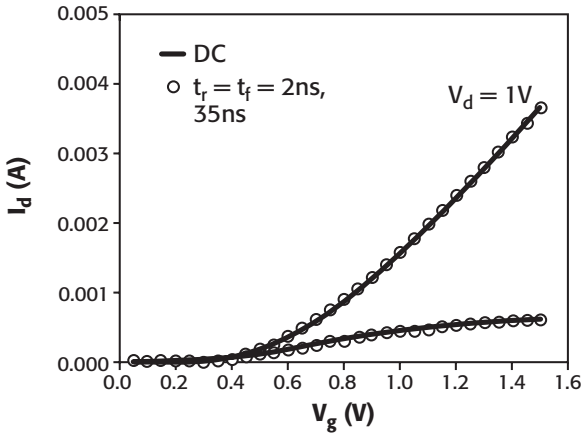


Figure 8. Overlay of V_{gs}-I_d curves between DC and pulse I-V measurement after calibration for transistor with SiO_2 gate.

However, device parasitics, usually parasitic capacitance between pad contacts, cannot be easily removed. This will reduce the pulse current from the drain terminal, as shown in ***Figure 3***. This problem can be designed out by using RF-compatible transistor structures (Ground-Signal-Ground), and by increasing pad pitch so that capacitance between the pads is small enough not to affect pulse current measurements.

Conclusion

DC characterization techniques are inadequate for capturing the dynamic nature of charge trapping in high κ gate stack structures. Pulse I-V is a powerful technique that allows characterizing transistors with high κ gate stacks in a trap-free environment that permits assessing their intrinsic qualities. With current measured in a shorter time than that associated with the charge-trapping time scale, improved intrinsic transistor characteristics can be achieved, including a drive current that is significantly higher than that measured with traditional DC I-V techniques.

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