# W83627HF/F

# WINBOND I/O

# W83627HF/F Data Sheet Revision History

|   | Pages | Dates | Version | Version on Web | Main Contents |
|---|---|---|---|---|---|
| 1 | n.a. | 09/25/98 | 0.50 | | Not released<br>For internal use only |
| 2 | 88-93,102,105, 139,151,153 | 11/10/98 | 0.51 | | First published.<br>Explanation of H/W Monitor function and<br>register correction. |
| 3 | 90-93;113-115 | 01/11/99 | 0.52 | | Pinout and register correction. |
| 4 | 90,91,113-115, 119-123,133,136, 137,140,141 | 07/26/99 | 0.53 | | Typo and data correction.<br>H/W Monitor register explanation. |
| 5 | All | 11/14/00 | 1.0 | 1.0 | New composition. |
| 6 | All | 11/01/02 | 2.0 | 2.0 | New composition. |
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## LIFE SUPPORT APPLICATIONS

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## GENERAL DESCRIPTION

The W83627HF and W83627F are evolving product from Winbond's most popular I/O family.  They feature a whole new interface, namely LPC (Low Pin Count) interface, which will be supported in the next generation Intel chip-set.   This interface as its name suggests is to provide an economical implementation of I/O's interface with lower pin count and still maintains equivalent performance as its ISA interface counterpart.   Approximately 40 pin counts are saved in LPC I/O comparing to ISA implementation.   With this additional freedom, we can implement more devices on a single chip as demonstrated in W83627F/HF's integration of Game Port and MIDI Port. It is fully transparent in terms of software which means no BIOS or device driver update is needed except chip-specific configuration.

The disk drive adapter functions of W83627F/HF include a floppy disk drive controller compatible with the industry standard 82077/ 765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic.  The wide range of functions integrated onto the W83627F/HF greatly reduces the number of components required for interfacing with floppy disk drives. The W83627F/HF supports four 360K, 720K, 1.2M, 1.44M, or 2.88M disk drives and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s,1 Mb/s, and 2 Mb/s.

The W83627F/HF provides two high-speed serial communication ports (UARTs), one of which supports serial Infrared communication.  Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and  a processor interrupt system.  Both UARTs provide legacy speed with baud rate up to 115.2k bps and also advanced speed with baud rates of  230k, 460k, or 921k bps which support higher speed modems. In addition, the W83627F/HF provides IR functions: IrDA 1.0 (SIR for 1.152K bps) and TV remote IR (Consumer IR, supporting NEC, RC-5, extended RC-5, and RECS-80 protocols).

The W83627F/HF supports one PC-compatible printer port (SPP), Bi-directional Printer port (BPP) and also Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP).  Through the printer port interface pins, also available are: Extension FDD Mode and Extension 2FDD Mode allowing one or two external floppy disk drives to be connected.

The configuration registers support mode selection, function enable/disable, and power down function selection.   Furthermore, the configurable PnP features are compatible with the plug-and-play feature demand of Windows 95/98$^{TM}$, which makes system resource allocation more efficient than ever.

The W83627F/HF provides functions that complies with ACPI (*Advanced Configuration and Power Interface*), which includes support of legacy and ACPI power management through  $PME\#$ or PSOUT# function pins. For OnNow keyboard Wake-Up, OnNow mouse Wake-Up, and OnNow CIR Wake-Up.  The W83627F/HF also has auto power management to reduce the power consumption.

The keyboard controller is based on 8042 compatible instruction set with a 2K Byte programmable ROM and a 256-Byte RAM bank.  Keyboard BIOS firmware are available with optional AMIKEY$^{TM}$-2, Phoenix MultiKey/42$^{TM}$, or customer code.

The W83627F/HF provides a set of flexible I/O control functions to the system designer through a set of General Purpose I/O ports. These GPIO ports may serve as simple I/O or may be individually configured to provide a predefined alternate function. General Purpose Port 1 is designed to be functional even in power down mode (VCC is off).

The W83627F/HF is made to fully comply with  Microsoft PC98 and PC99 Hardware Design Guide. Moreover W83627F/HF is made to meet the specification of PC98/PC99's requirement in the power management: ACPI and DPM (Device Power Management).

The W83627F/HF contains a game port and a MIDI port. The game port is designed to support 2 joysticks and can be applied to all standard PC game control devices, They are very important for a entertainment or consumer computer.

Only the W83627HF support hardware status monitoring for personal computers. It can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system to work stably and properly.

## FEATURES

### General

- Meet LPC Spec. 1.0
- Support LDRQ#(LPC DMA), SERIRQ (serial IRQ)
- Include all the features of Winbond I/O W83977TF and W83977EF
- Integrate Hardware Monitor functions
- Compliant with Microsoft PC98/PC99 Hardware Design Guide
- Support DPM (Device Power Management), ACPI
- Programmable configuration settings
- Single 24 or 48 MHz clock input

### FDC

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track selectable capability
- Support vertical recording format
- DMA enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detects all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD write enable signal (write data signal was forced to be inactive)
- Support up to four 3.5-inch or 5.25-inch floppy disk drives
- Completely compatible with industry standard 82077
- 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Support 3-mode FDD, and its Win95/98 driver

## UART

- Two high-speed 16550 compatible UARTs with 16-byte send/receive FIFOs

- MIDI compatible

- Fully programmable serial-interface characteristics:

  --- 5, 6, 7 or 8-bit characters

  --- Even, odd or no parity bit generation/detection

  --- 1, 1.5 or 2 stop bits generation

- Internal diagnostic capabilities:

  --- Loop-back controls for communications link fault isolation

  --- Break, parity, overrun, framing error simulation

- Programmable baud generator allows division of 1.8461 MHz and 24 MHz by 1 to ($2^{16}$-1)

- Maximum baud rate up to 921k bps for 14.769 MHz and 1.5M bps for 24 MHz

## Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps

- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps

- Support Consumer IR

## Parallel Port

- Compatible with IBM parallel port

- Support PS/2 compatible bi-directional parallel port

- Support Enhanced Parallel Port (EPP) − Compatible with IEEE 1284 specification

- Support Extended Capabilities Port (ECP) − Compatible with IEEE 1284 specification

- Extension FDD mode supports disk drive B; and Extension 2FDD mode supports disk drives A and B through parallel port

- Enhanced printer port back-drive current protection

## Keyboard Controller

- 8042 based with optional F/W from AMIKKEY$^{TM}$-2, Phoenix MultiKey/42$^{TM}$ or customer code with 2K bytes of programmable ROM, and 256 bytes of RAM

- Asynchronous Access to Two Data Registers and One status Register

- Software compatibility with the 8042

- Support PS/2 mouse

- Support port 92
- Support both interrupt and polling modes
- Fast Gate A20 and Hardware Keyboard Reset
- 8 Bit Timer/ Counter
- Support binary and BCD arithmetic
- 6 MHz, 8 MHz, 12 MHz, or 16 MHz operating frequency

**Game Port**

- Support two separate Joysticks
- Support every Joystick two axis (X,Y) and two button (A,B) controllers

**MIDI Port**

- The baud rate is 31.25 Kbaud
- 16-byte input FIFO
- 16-byte output FIFO

**General Purpose I/O Ports**

- 22 programmable general purpose I/O ports
- General purpose I/O ports can serve as simple I/O ports, interrupt steering inputs, watch dog timer output, power LED output, infrared I/O pins, KBC control I/O pins, suspend LED output, RSMRST# signal, PWROK signal, Beep output
- Functional in power down mode (GP1 only)

**OnNow Functions**

- Keyboard Wake-Up by programmable keys
- Mouse Wake-Up by programmable buttons
- CIR Wake-Up by programmable keys
- On Now Wake-Up from all of the ACPI sleeping states (S1-S5)

**Hardware Monitor Functions ( Only for W83627HF)**

- 5 VID input pins for CPU Vcore identification
- 3 thermal inputs from optionally remote thermistors or 2N3904 transistors or Pentium$^{TM}$ II (Deschutes) thermal diode output
- 7 positive voltage inputs (typical for +12V, -12V, +5V, -5V, +3.3V, VcoreA, VcoreB)
- 2 intrinsic voltage monitoring (typical for Vbat, +5VSB)

- 3 fan speed monitoring inputs

- 2 fan speed control

- Build in Case open detection circuit

- WATCHDOG comparison of all monitored values

- Programmable hysteresis and setting points for all monitored items

- Over temperature indicate output

- Automatic Power On voltage detection Beep

- Issue SMI#, IRQ, OVT# to activate system protection

- Intel LDCM$^{TM}$ / Acer ADM$^{TM}$ compatible

## Package
- 128-pin PQFP

## PIN CONFIGURATION FOR 627F

W83627F

Left side pins:
- 103 NC
- 104 NC
- 105 NC
- 106 NC
- 107 NC
- 108 NC
- 109 NC
- 110 NC
- 111 NC
- 112 NC
- 113 NC
- 114 VCC
- 115 NC
- 116 NC
- 117 VSS
- 118 NC
- 119 MSI/GP20
- 120 MSO/IRQIN0
- 121 GPSA2/GP17
- 122 GPSB2/GP16
- 123 GPY1/GP15
- 124 GPY2/P16/GP14
- 125 GPX2/P15/GP13
- 126 GPX1/P14/GP12
- 127 GPSB1/P13/GP11
- 128 GPSA1/P12/GP10

Right side pins:
- 64 SUSLED/GP35
- 63 KDAT
- 62 KCLK
- 61 VSB
- 60 KBRST
- 59 A20GATE
- 58 KBLOCK#
- 57 RIA#
- 56 DCDA#
- 55 VSS
- 54 SOUTA
- 53 SINA
- 52 DTRA#
- 51 RTSA#
- 50 DSRA#
- 49 CTSA#
- 48 VCC
- 47 STB#
- 46 AFD#
- 45 ERR#
- 44 INIT#
- 43 SLIN#
- 42 PD0
- 41 PD1
- 40 PD2
- 39 PD3

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## PIN CONFIGURATION FOR 627HF

W83627HF

| Pin | Left signal |
|-----|-------------|
| 103 | VTIN2 |
| 104 | VTIN1 |
| 105 | OVT# |
| 106 | VID4 |
| 107 | VID3 |
| 108 | VID2 |
| 109 | VID1 |
| 110 | VID0 |
| 111 | FANIO3 |
| 112 | FANIO2 |
| 113 | FANIO1 |
| 114 | VCC |
| 115 | FANPWM2 |
| 116 | FANPWM1 |
| 117 | VSS |
| 118 | BEEP |
| 119 | MSI/GP20 |
| 120 | MSO/IRQIN0 |
| 121 | GPSA2/GP17 |
| 122 | GPSB2/GP16 |
| 123 | GPY1/GP15 |
| 124 | GPY2/P16/GP14 |
| 125 | GPX2/P15/GP13 |
| 126 | GPX1/P14/GP12 |
| 127 | GPSB1/P13/GP11 |
| 128 | GPSA1/P12/GP10 |

| Pin | Right signal |
|-----|--------------|
| 64 | SUSLED/GP35 |
| 63 | KDAT |
| 62 | KCLK |
| 61 | VSB |
| 60 | KBRST |
| 59 | A20GATE |
| 58 | KBLOCK# |
| 57 | RIA# |
| 56 | DCDA# |
| 55 | VSS |
| 54 | SOUTA |
| 53 | SINA |
| 52 | DTRA# |
| 51 | RTSA# |
| 50 | DSRA# |
| 49 | CTSA# |
| 48 | VCC |
| 47 | STB# |
| 46 | AFD# |
| 45 | ERR# |
| 44 | INIT# |
| 43 | SLIN# |
| 42 | PD0 |
| 41 | PD1 |
| 40 | PD2 |
| 39 | PD3 |

# 1. PIN  DESCRIPTION

Note: Please refer to Section 5.2  DC CHARACTERISTICS for details

| PIN  DESCRIPTION | |
|---|---|
| I/O$_{8t}$ | TTL level bi-directional pin with 8mA source-sink capability |
| I/O$_{12t}$ | TTL level bi-directional pin with 12mA source-sink capability |
| I/O$_{24t}$ | TTL level bi-directional pin with 24 mA source-sink capability |
| I/O$_{12tp3}$ | 3.3V TTL level bi-directional pin with 12mA source-sink capability |
| I/O$_{12ts}$ | TTL level Schmitt-trigger bi-directional pin with 12mA source-sink capability |
| I/O$_{24ts}$ | TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability |
| I/O$_{24tsp3}$ | 3.3V TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability |
| I/OD$_{12t}$ | TTL level bi-directional pin and open-drain output with 12mA sink capability |
| I/OD$_{24t}$ | TTL level bi-directional pin and open-drain output with 24mA sink capability |
| I/OD$_{12ts}$ | TTL level Schmitt-trigger bi-directional pin and open-drain output with 12mA sink capability |
| I/OD$_{24ts}$ | TTL level Schmitt-trigger bi-directional pin and open-drain output with 24mA sink capability |
| I/OD$_{12cs}$ | CMOS level Schmitt-trigger bi-directional pin and open-drain output with 12mA sink capability |
| I/OD$_{16cs}$ | CMOS level Schmitt-trigger bi-directional pin and open-drain output with 16mA sink capability |
| I/OD$_{12csd}$ | CMOS level Schmitt-trigger bi-directional pin with internal pull down resistor and open-drain output with 12mA sink capability |
| I/OD$_{12csu}$ | CMOS level Schmitt-trigger bi-directional pin with internal pull up resistor and open-drain output with 12mA sink capability |
| O$_4$ | Output pin with 4 mA source-sink capability |
| O$_8$ | Output pin with 8 mA source-sink capability |
| O$_{12}$ | Output pin with 12 mA source-sink capability |
| O$_{16}$ | Output pin with 16 mA source-sink capability |
| O$_{24}$ | Output pin with 24 mA source-sink capability |
| O$_{12p3}$ | 3.3V output pin with 12 mA source-sink capability |
| O$_{24p3}$ | 3.3V output pin with 24 mA source-sink capability |
| OD$_{12}$ | Open-drain output pin with 12 mA sink capability |
| OD$_{24}$ | Open-drain output pin with 24 mA sink capability |
| OD$_{12p3}$ | 3.3V open-drain output pin with 12 mA sink capability |
| IN$_t$ | TTL level input pin |
| IN$_{tp3}$ | 3.3V TTL level input pin |
| IN$_{td}$ | TTL level input pin with internal pull down resistor |
| IN$_{tu}$ | TTL level input pin with internal pull up resistor |
| IN$_{ts}$ | TTL level Schmitt-trigger input pin |
| IN$_{tsp3}$ | 3.3V TTL level Schmitt-trigger input pin |
| IN$_c$ | CMOS level input pin |
| IN$_{cd}$ | CMOS level input pin with internal pull down resistor |
| IN$_{cs}$ | CMOS level Schmitt-trigger input pin |
| IN$_{csu}$ | CMOS level Schmitt-trigger input pin with internal pull up resistor |

## 1.1 LPC Interface

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| CLKIN | 18 | $IN_{t3}$ | System clock input. According to the input frequency 24MHz or 48MHz, it is selectable through register. Default is 24MHz input. |
| PME# | 19 | $OD_{12p3}$ | Generated PME event. |
| PCICLK | 21 | $IN_{tsp3}$ | PCI clock input. |
| LDRQ# | 22 | $O_{12p3}$ | Encoded DMA Request signal. |
| SERIRQ | 23 | $I/O_{12tp3}$ | Serial IRQ input/Output. |
| LAD[3:0] | 24-27 | $I/O_{12tp3}$ | These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral. |
| LFRAME# | 29 | $IN_{tsp3}$ | Indicates start of a new cycle or termination of a broken cycle. |
| LRESET# | 30 | $IN_{tsp3}$ | Reset signal. It can connect to PCIRST# signal on the host. |
| SUSCLKIN | 75 | $IN_{tsp3}$ | 32khz clock input , for CIR only. |

## 1.2 FDC Interface

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| DRVDEN0 | 1 | $OD_{24}$ | Drive Density Select bit 0. |
| DRVDEN1 | 2 | OD24 | Drive Density Select bit 1. (Default) |
| SMI# | | OD24 | System Management Interrupt |
| (IRQIN1) | | INt | (Interrupt channel input. For C version only) |
| GP27 | | I/OD24t | General purpose I/O port 3 bit 6. |
| INDEX# | 3 | $IN_{csu}$ | This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. This input pin is pulled up internally by a 1 K  resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN). |
| MOA# | 4 | $OD_{24}$ | Motor A On. When set to 0, this pin enables disk drive 0.  This is an open drain output. |

1.2 FDC Interface continued

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| DSB#<br><br>FANIN3 | 5 | OD$_{24}$<br><br>I/O$_{24ts}$ | Drive Select B. When set to 0, this pin enables disk drive B.  This is an open drain output.<br>0V to +5V amplitude fan tachometer input |
| DSA# | 6 | OD$_{24}$ | Drive Select A. When set to 0, this pin enables disk drive A.  This is an open drain output. |
| MOB#<br><br>FANPWM3 | 7 | OD$_{24}$<br><br>OD$_{24}$ | Motor B On. When set to 0, this pin enables disk drive 1. This is an open drain output.<br>Fan speed control. Use the Pulse Width Modulation (PWM) technical knowledge to control the Fan's RPM. |
| DIR# | 8 | OD$_{24}$ | Direction of the head step motor. An open drain output.<br>Logic 1 = outward motion<br>Logic 0 = inward motion |
| STEP# | 9 | OD$_{24}$ | Step output pulses. This active low open drain output produces a pulse to move the head to another track. |
| WD# | 10 | OD$_{24}$ | Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output. |
| WE# | 11 | OD$_{24}$ | Write enable. An open drain output. |
| TRACK0# | 13 | IN$_{csu}$ | Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track. This input pin is pulled up internally by a 1 K  resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN). |
| WP# | 14 | IN$_{csu}$ | Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin is pulled up internally by a 1 K  resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN). |
| RDATA# | 15 | IN$_{csu}$ | The read data input signal from the FDD. This input pin is pulled up internally by a 1 K  resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN). |
| HEAD# | 16 | OD24 | Head select. This open drain output determines which dsk drive head is active.<br>Logic 1 = side 0<br>Logic 0 = side 1 |
| DSKCHG# | 17 | IN$_{csu}$ | Diskette change. This signal is active low at power on and whenever the diskette is removed. This input pin is pulled up internally by a 1 K  resistor.  The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN). |

## 1.3 Multi-Mode Parallel Port

The following pins have alternate functions, which are controlled by CR28 and L3-CRF0.

| SYMBOL | PIN | I/O | FUNCTION |
|--------|-----|-----|----------|
| SLCT<br><br>WE2# | 31 | $IN_{ts}$<br><br>$OD_{12}$ | PRINTER MODE:<br><br>An active high input on this pin indicates that the printer is selected. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.<br><br>EXTENSION FDD MODE: WE2#<br><br>This pin is for Extension FDD B; its function is the same as the WE# pin of FDC.<br><br>EXTENSION 2FDD MODE: WE2#<br><br>This pin is for Extension FDD A and B; its function is the same as the WE# pin of FDC. |
| PE<br><br>WD2# | 32 | $IN_{ts}$<br><br>$OD_{12}$ | PRINTER MODE:<br><br>An active high input on this pin indicates that the printer has detected the end of the paper. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.<br><br>EXTENSION FDD MODE: WD2#<br><br>This pin is for Extension FDD B; its function is the same as the WD# pin of FDC.<br><br>EXTENSION 2FDD MODE: WD2#<br><br>This pin is for Extension FDD A and B; its function is the same as the WD# pin of FDC. |

1.3 Multi-Mode Parallel Port, continued

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| BUSY<br><br><br>MOB2# | 33 | $IN_{ts}$<br><br><br><br>$OD_{12}$ | PRINTER MODE:<br><br>An active high input indicates that the printer is not ready to receive data. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.<br><br>EXTENSION FDD MODE: MOB2#<br><br>This pin is for Extension FDD B; its function is the same as the MOB# pin of FDC.<br><br>EXTENSION 2FDD MODE: MOB2#<br><br>This pin is for Extension FDD A and B; its function is the same as the MOB# pin of FDC. |
| ACK#<br><br><br><br><br>DSB2# | 34 | $IN_{ts}$<br><br><br><br><br><br>$OD_{12}$ | PRINTER MODE: ACK#<br><br>An active low input on this pin indicates that the printer has received data and is ready to accept more data. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.<br><br>EXTENSION FDD MODE: DSB2#<br><br>This pin is for the Extension FDD B; its functions is the same as the DSB# pin of FDC.<br><br>EXTENSION 2FDD MODE: DSB2#<br><br>This pin is for Extension FDD A and B; its function is the same as the DSB# pin of FDC. |
| PD7<br><br><br>DSA2# | 35 | $I/O_{12ts}$<br><br><br><br>$OD_{12}$ | PRINTER MODE: PD7<br><br>Parallel port data bus bit 7.  Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.<br><br>EXTENSION FDD MODE: This pin is a tri-state output.<br><br>EXTENSION 2FDD MODE: DSA2#<br><br>This pin is for Extension FDD A; its function is the same as the DSA# pin of FDC. |
| PD6<br><br><br>MOA2# | 36 | $I/O_{12ts}$<br><br><br><br>$OD_{12}$ | PRINTER MODE: PD6<br><br>Parallel port data bus bit 6.  Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.<br><br>EXTENSION FDD MODE: This pin is a tri-state output.<br><br>EXTENSION. 2FDD MODE: MOA2#<br><br>This pin is for Extension FDD A; its function is the same as the MOA# pin of FDC. |

1.3 Multi-Mode Parallel Port, continued

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| PD5 | 37 | I/O$_{12ts}$ | PRINTER MODE: PD5 |
| | | | Parallel port data bus bit 5.   Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| | | | EXTENSION FDD MODE: This pin is a tri-state output. |
| | | | EXTENSION 2FDD MODE: This pin is a tri-state output. |
| PD4 | 38 | I/O$_{12ts}$ | PRINTER MODE: PD4 |
| | | | Parallel port data bus bit 4.  Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| DSKCHG2# | | IN$_{ts}$ | EXTENSION FDD MODE: DSKCHG2# |
| | | | This pin is for Extension FDD B; the function of this pin is the same as the DSKCHG# pin of FDC.  It is pulled high internally. |
| | | | EXTENSION 2FDD MODE: DSKCHG2# |
| | | | This pin is for Extension FDD A and B; this function of this pin is the same as the DSKCHG# pin of FDC.  It is pulled high internally. |
| PD3 | 39 | I/O$_{12ts}$ | PRINTER MODE: PD3 |
| | | | Parallel port data bus bit 3.  Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| RDATA2# | | IN$_{ts}$ | EXTENSION FDD MODE: RDATA2# |
| | | | This pin is for Extension FDD B; its function is the same as the RDATA# pin of FDC.  It is pulled high internally. |
| | | | EXTENSION 2FDD MODE: RDATA2# |
| | | | This pin is for Extension FDD A and B; its function is the same as the RDATA# pin of FDC.  It is pulled high internally. |
| PD2 | 40 | I/O$_{12ts}$ | PRINTER MODE: PD2 |
| | | | Parallel port data bus bit 2.  Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| WP2# | | IN$_{ts}$ | EXTENSION FDD MODE: WP2# |
| | | | This pin is for Extension FDD B; its function is the same as the WP# pin of FDC.  It is pulled high internally. |
| | | | EXTENSION. 2FDD MODE: WP2# |
| | | | This pin is for Extension FDD A and B; its function is the same as the WP# pin of FDC.  It is pulled high internally. |

1.3 Multi-Mode Parallel Port, continued

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| PD1<br><br>TRAK02# | 41 | I/O$_{12ts}$<br><br><br>IN$_{ts}$ | PRINTER MODE: PD1<br>Parallel port data bus bit 1.  Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.<br>EXTENSION FDD MODE: TRAK02#<br>This pin is for Extension FDD B; its function is the same as the TRAK0# pin of FDC.  It is pulled high internally.<br>EXTENSION. 2FDD MODE: TRAK02#<br>This pin is for Extension FDD A and B; its function is the same as the TRAK0# pin of FDC.  It is pulled high internally. |
| PD0<br><br><br>INDEX2# | 42 | I/O$_{12ts}$<br><br><br><br>IN$_{ts}$ | PRINTER MODE: PD0<br>Parallel port data bus bit 0.  Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.<br><br>EXTENSION FDD MODE: INDEX2#<br>This pin is for Extension FDD B; its function is the same as the INDEX# pin of FDC.  It is pulled high internally.<br><br>EXTENSION 2FDD MODE: INDEX2#<br>This pin is for Extension FDD A and B; its function is the same as the INDEX# pin of FDC.  It is pulled high internally. |
| SLIN#<br><br><br><br>STEP2# | 43 | OD$_{12}$<br><br><br><br><br>OD$_{12}$ | PRINTER MODE: SLIN#<br>Output line for detection of printer selection. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.<br>EXTENSION FDD MODE: STEP2#<br>This pin is for Extension FDD B; its function is the same as the STEP# pin of FDC.<br>EXTENSION 2FDD MODE: STEP2#<br>This pin is for Extension FDD A and B; its function is the same as the STEP# pin of FDC. |
| INIT#<br><br><br><br>DIR2# | 44 | OD$_{12}$<br><br><br><br><br>OD$_{12}$ | PRINTER MODE: INIT#<br>Output line for the printer initialization. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.<br>EXTENSION FDD MODE: DIR2#<br>This pin is for Extension FDD B; its function is the same as the DIR# pin of FDC.<br>EXTENSION 2FDD MODE: DIR2#<br>This pin is for Extension FDD A and B; its function is the same as the DIR# pin of FDC. |

1.3 Multi-Mode Parallel Port, continued

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| ERR#<br><br><br>HEAD2# | 45 | IN$_{ts}$<br><br><br>OD$_{12}$ | PRINTER MODE: ERR#<br><br>An active low input on this pin indicates that the printer has encountered an error condition. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.<br>EXTENSION FDD MODE: HEAD2#<br><br>This pin is for Extension FDD B; its function is the same as the HEAD# pin of FDC.<br>EXTENSION 2FDD MODE: HEAD2#<br><br>This pin is for Extension FDD A and B; its function is the same as the HEAD# pin of FDC. |
| AFD#<br><br><br>DRVDEN0 | 46 | OD$_{12}$<br><br><br>OD$_{12}$ | PRINTER MODE: AFD#<br><br>An active low output from this pin causes the printer to auto feed a line after a line is printed. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.<br>EXTENSION FDD MODE: DRVDEN0<br><br>This pin is for Extension FDD B; its function is the same as the DRVDEN0 pin of FDC.<br>EXTENSION 2FDD MODE: DRVDEN0<br><br>This pin is for Extension FDD A and B; its function is the same as the DRVDEN0 pin of FDC. |
| STB# | 47 | OD$_{12}$ | PRINTER MODE: STB#<br>An active low output is used to latch the parallel data into the printer. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.<br><br>EXTENSION FDD MODE: This pin is a tri-state output<br>EXTENSION 2FDD MODE: This pin is a tri-state output. |

# W83627HF/F

## 1.4 Serial Port Interface

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| CTSA#<br>CTSB# | 49<br>78 | IN$_t$ | Clear To Send. It is the modem control input.<br>The function of these pins can be tested by reading bit 4 of the handshake status register. |
| DSRA#<br>DSRB# | 50<br>79 | IN$_t$ | Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART. |
| RTSA#<br><br>HEFRAS | 51 | O$_{8C}$<br><br>IN$_{cd}$ | UART A Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.<br>During power-on reset, this pin is pulled down internally and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 (HEFRAS). A 4.7 k$\Omega$ is recommended if intends to pull up. (select 4EH as configuration I/O port's address) |
| DTRA#<br><br>PNPCVS# | 52 | O$_{8C}$<br><br>IN$_{cd}$ | UART B Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.<br>During power-on reset, this pin is pulled down internally and is defined as PNPCVS# , which provides the power-on value for CR24 bit 0, A 4.7k$\Omega$ is recommended if intends to pull up.(This bit is used to clear the default value of FDC, UARTs, and LPT setting) |
| RTSB# | 80 | O$_{8C}$ | UART B Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. |
| DTRB# | 81 | O$_{8C}$ | UART B Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate. |
| SINA<br>SINB | 53<br>82 | IN$_t$ | Serial Input. It is used to receive serial data through the communication link. |
| SOUTA<br><br>PENKBC | 54 | O$_{8C}$<br><br>IN$_{cd}$ | UART A Serial Output. It is used to transmit serial data out to the communication link.<br>During power-on reset, this pin is pulled down internally and is defined as PENKBC, which provides the power-on value for CR24 bit 2 (PENKBC). A 4.7 k$\Omega$ resistor is recommended if intends to pull up. ( enable KBC) |
| SOUTB<br><br>PEN48 | 83 | O$_{8C}$<br><br>IN$_{cd}$ | UART B Serial Output. During power-on reset, this pin is pulled down internally and is defined as PEN48, which provides the power-on value for CR24 bit 6 (EN48). A 4.7 k$\Omega$ resistor is recommended if intends to pull up. |
| DCDA#<br>DCDB# | 56<br>84 | IN$_t$ | Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier. |
| RIA#<br>RIB# | 57<br>85 | IN$_t$ | Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set. |

## 1.5 KBC Interface

| SYMBOL | PIN | I/O | FUNCTION |
|--------|-----|-----|----------|
| KBLOCK# | 58 | $IN_t$ | Keyboard inhibit control input. This pin is after system reset. Internal pull high. (KBC P17) |
| GA20M | 59 | $O_{16}$ | Gate A20 output. This pin is high after system reset. (KBC P21) |
| KBRST | 60 | $O_{16}$ | Keyboard reset. This pin is high after system reset. (KBC P20) |
| KCLK | 62 | $I/OD_{16cs}$ | Keyboard Clock. |
| KDAT | 63 | $I/OD_{16cs}$ | Keyboard Data. |
| MCLK | 65 | $I/OD_{16cs}$ | PS2 Mouse Clock. |
| MDAT | 66 | $I/OD_{16cs}$ | PS2 Mouse Data. |

## 1.6 ACPI Interface

| SYMBOL | PIN | I/O | FUNCTION |
|--------|-----|-----|----------|
| PSOUT# | 67 | $OD_{12}$ | Panel Switch Output. This signal is used for Wake-Up system from $S5_{cold}$ state. This pin is pulse output, active low. |
| PSIN | 68 | $IN_{cd}$ | Panel Switch Input. This pin is high active with an internal pull down resistor. |
| VBAT | 74 | PWR | Battery voltage input. |

## 1.7 Hardware Monitor Interface

(For W83627HF only, all these pins in W83627F are NC.)

| SYMBOL | PIN | I/O | FUNCTION |
|--------|-----|-----|----------|
| CASEOPEN# | 76 | $IN_t$ | CASE OPEN. An active low input from an external device when case is opened. This signal can be latched if pin VBAT is connect to battery, even W83627HF is power off. |
| -5VIN | 94 | AIN | 0V to 4.096V FSR Analog Inputs. |
| -12VIN | 95 | AIN | 0V to 4.096V FSR Analog Inputs. |
| +12VIN | 96 | AIN | 0V to 4.096V FSR Analog Inputs. |
| +3.3VIN | 98 | AIN | 0V to 4.096V FSR Analog Inputs. |
| VCOREB | 99 | AIN | 0V to 4.096V FSR Analog Inputs. |
| VCOREA | 100 | AIN | 0V to 4.096V FSR Analog Inputs. |
| VREF | 101 | PWR | Reference Voltage for temperature measuration. |
| VTIN2 | 103 | AIN | Temperature sensor 2 input. It is used for CPU1 temperature measuration. |
| VTIN1 | 104 | AIN | Temperature sensor 1 input. It is used for system temperature measuration. |

1.7 Hardware Monitor Interface, continued

| SYMBOL | PIN | I/O | FUNCTION |
|--------|-----|-----|----------|
| OVT# | 105 | $OD_{24}$ | Over temperature Shutdown Output. It indicated the VTIN2 or VTIN3 is over temperature limit. |
| VID[4:0] | 106-110 | $IN_t$ | Voltage Supply readouts from Pentium II . |
| FANIO[3:1] | 111-113 | $I/O_{12ts}$ | 0V to +5V amplitude fan tachometer input. Alternate Function: Fan on-off control output. These multifunctional pins can be programmable input or output. |
| FANPWM1 FANPWM2 | 116 115 | $O_{12}$ | Fan speed control. Use the Pulse Width Modulatuion (PWM) technic knowledge to control the Fan's RPM. |
| BEEP | 118 | OD12 | Beep function for hardware monitor. This pin is low after system reset. |

## 1.8 Game Port & MIDI Port

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| MSI | 119 | INtu | MIDI serial data input .(Default) |
| GP20 | | I/OD$_{12t}$ | General purpose I/O port 2 bit 0. |
| MSO | 120 | O$_8$C | MIDI serial data output. (Default) |
| IRQIN0 | | INc | Alternate Function input: Interrupt channel input. |
| GPSA2 | 121 | INcsu | Active-low, Joystick I switch input 2. This pin has an internal pull-up resistor. (Default) |
| GP17 | | I/OD$_{12csu}$ | General purpose I/O port 1 bit 7. |
| GPSB2 | 122 | INcsu | Active-low, Joystick II switch input 2. This pin has an internal pull-up resistor. (Default) |
| GP16 | | I/OD$_{12csu}$ | General purpose I/O port 1 bit 6. |
| GPY1 | 123 | I/OD$_{12csd}$ | Joystick I timer pin. This pin connects to Y positioning variable resistors for the Joystick. (Default) |
| GP15 | | I/OD$_{12cs}$ | General purpose I/O port 1 bit 5. |
| GPY2 | 124 | I/OD$_{12csd}$ | Joystick II timer pin. This pin connects to Y positioning variable resistors for the Joystick. (Default) |
| GP14 | | I/OD$_{12cs}$ | General purpose I/O port 1 bit 4. |
| P16 | | | Alternate Function Output: KBC P16 I/O port. |
| GPX2 | 125 | I/OD$_{12csd}$ | Joystick II timer pin. This pin connects to X positioning variable resistors for the Joystick. (Default) |
| GP13 | | I/OD$_{12cs}$ | General purpose I/O port 1 bit 3. |
| P15 | | | Alternate Function Output: KBC P15 I/O port. |
| GPX1 | 126 | I/OD$_{12csd}$ | Joystick I timer pin. This pin connects to X positioning variable resistors for the Joystick. (Default) |
| GP12 | | I/OD$_{12cs}$ | |
| P14 | | | General purpose I/O port 1 bit 2. |
| | | | Alternate Function Output: KBC P14 I/O port. |
| GPSB1 | 127 | INcsu | Active-low, Joystick II switch input 1. (Default) |
| GP11 | | I/OD$_{12csu}$ | General purpose I/O port 1 bit 1. |
| P13 | | | Alternate Function Output: KBC P13 I/O port. |
| GPSA1 | 128 | INcsu | Active-low, Joystick I switch input 1. (Default) |
| GP10 | | I/OD$_{12csu}$ | General purpose I/O port 1 bit 0. |
| P12 | | | Alternate Function Output: KBC P12 I/O port. |

## 1.9 General Purpose I/O Port

### 1.9.1 General Purpose I/O Port 1 (Power source is Vcc)

see 1.8 Game Port

### 1.9.2 General Purpose I/O Port 2 (Power source is Vcc)

| SYMBOL | PIN | I/O | FUNCTION |
|--------|-----|-----|----------|
| GP20 | 119 | I/OD$_{12t}$ | General purpose I/O port 2 bit 0. |
| GP21 | 92 | I/OD$_{12t}$ | General purpose I/O port 2 bit 1. |
| GP22 | 91 | I/OD$_{12t}$ | General purpose I/O port 2 bit 2. |
| GP23 | 90 | I/OD$_{24t}$ | General purpose I/O port 2 bit 3. |
| GP24 | 89 | I/OD$_{12t}$ | General purpose I/O port 2 bit 4. |
| GP25 | 88 | I/OD$_{12t}$ | General purpose I/O port 2 bit 5. |
| GP26 | 87 | I/OD$_{12t}$ | General purpose I/O port 2 bit 6. |
| GP27 | 2 | I/OD$_{24t}$ | General purpose I/O port 2 bit 7. |

## 1.9.3 General Purpose I/O Port 3 (Power souce is VSB)

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| GP30 | 73 | I/OD$_{12t}$ | General purpose I/O port 3 bit 0. |
| SLP_SX# | | IN$_{ts}$ | Chpset suspend C status input. |
| GP31 | 72 | I/OD$_{12t}$ | General purpose I/O port 3 bit 1. |
| PWRCTL# | | O$_{12}$ | This pin generates the PWRCTL# signal while the power failure. (Default) |
| GP32 | 71 | I/OD$_{12t}$ | General purpose I/O port 3 bit 2. |
| PWROK | | OD$_{12}$ | This pin generates the PWROK signal while the VCC come in. (Default) |
| GP33 | 70 | I/OD$_{12t}$ | General purpose I/O port 3 bit 3. |
| RSMRST# | | OD$_{12}$ | This pin generates the RSMRST signal while the VSB come in. (Default) |
| GP34 | 69 | I/OD$_{12t}$ | General purpose I/O port 3 bit 4. |
| CIRRX# | | IN$_{ts}$ | Consumer IR receiving input. This pin can Wake-Up system from S5$_{cold}$. (Default) |
| GP35 | 64 | I/OD$_{24t}$ | General purpose I/O port 3 bit 5. |
| SUSLED | | O$_{24}$ | Suspend LED output, it can program to flash when suspend state. This function can work without VCC. (Default) |

## 1.10 POWER PINS

| SYMBOL | PIN | FUNCTION |
|---|---|---|
| VCC | 12, 48, 77, 114 | +5V power supply for the digital circuitry. |
| VSB | 61 | +5V stand-by power supply for the digital circuitry. |
| VCC3V | 28 | +3.3V power supply for driving 3V on host interface. |
| AVCC | 97 | Analog VCC input. Internally supplier to all analog circuitry. |
| AGND | 93 | Internally connected to all analog circuitry. The ground reference for all analog inputs.. |
| VSS | 20, 55, 86, 117 | Ground. |

## 2. HARDWARE MONITOR

### 2.1 General Description

The W83627HF  can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system to work stable and properly.  W83627HF provides both LPC and I²C™ serial bus interface to access hardware .

An 8-bit analog-to-digital converter (ADC) was built inside W83627HF.  The W83627HF can simultaneously monitor 9 analog voltage inputs, 3 fan tachometer inputs, 3 remote temperature, one case-open detection signal.  The remote temperature sensing can be performed by thermistors, or 2N3904 NPN-type transistors, or directly from Intel™ Deschutes CPU thermal diode output.  Also the W83627HF provides: 2 PWM (pulse width modulation) outputs for the fan speed control; beep tone output for warning; SMI#(through serial IRQ) , OVT#, GPO# signals for system protection events.

Through the application software or BIOS, the users can read all the monitored parameters of system from time to time.  And a pop-up warning can be also activated when the monitored item was out of the proper/preset range.  The application software could be Winbond's Hardware Doctor™, or Intel™ LDCM (LanDesk Client Management), or other management application software.  Also the users can set up the upper and lower limits (alarm thresholds) of these monitored parameters and to activate one programmable and maskable interrupts.  An optional beep tone could be used as warning signal when the monitored parameters is out of the preset range.

Additionally, 5 VID inputs are provided to read the VID of CPU (i.e. Pentium™ II) if applicable. This is to provide the Vcore voltage correction automatically.  Also W83627HF uniquely provides an optional feature: early stage (before BIOS was loaded) beep warning. This is to detect if the fatal elements present --- Vcore or +3.3V voltage fail, and the system can not be boomed up.

### 2.2 Access Interface

The W83627HF provides two interface for microprocessor to read/write hardware monitor internal registers.

#### 2.2.1 LPC interface

The first interface uses LPC Bus to access which the ports of low byte (bit2~bit0) are defined in the port 5h and 6h. The other higher bits of these ports is set by W83627HF itself.  The general decoded address is set to port 295h and port 296h. These two ports are described as following:

Port 295h: Index port.

Port 296h: Data port.

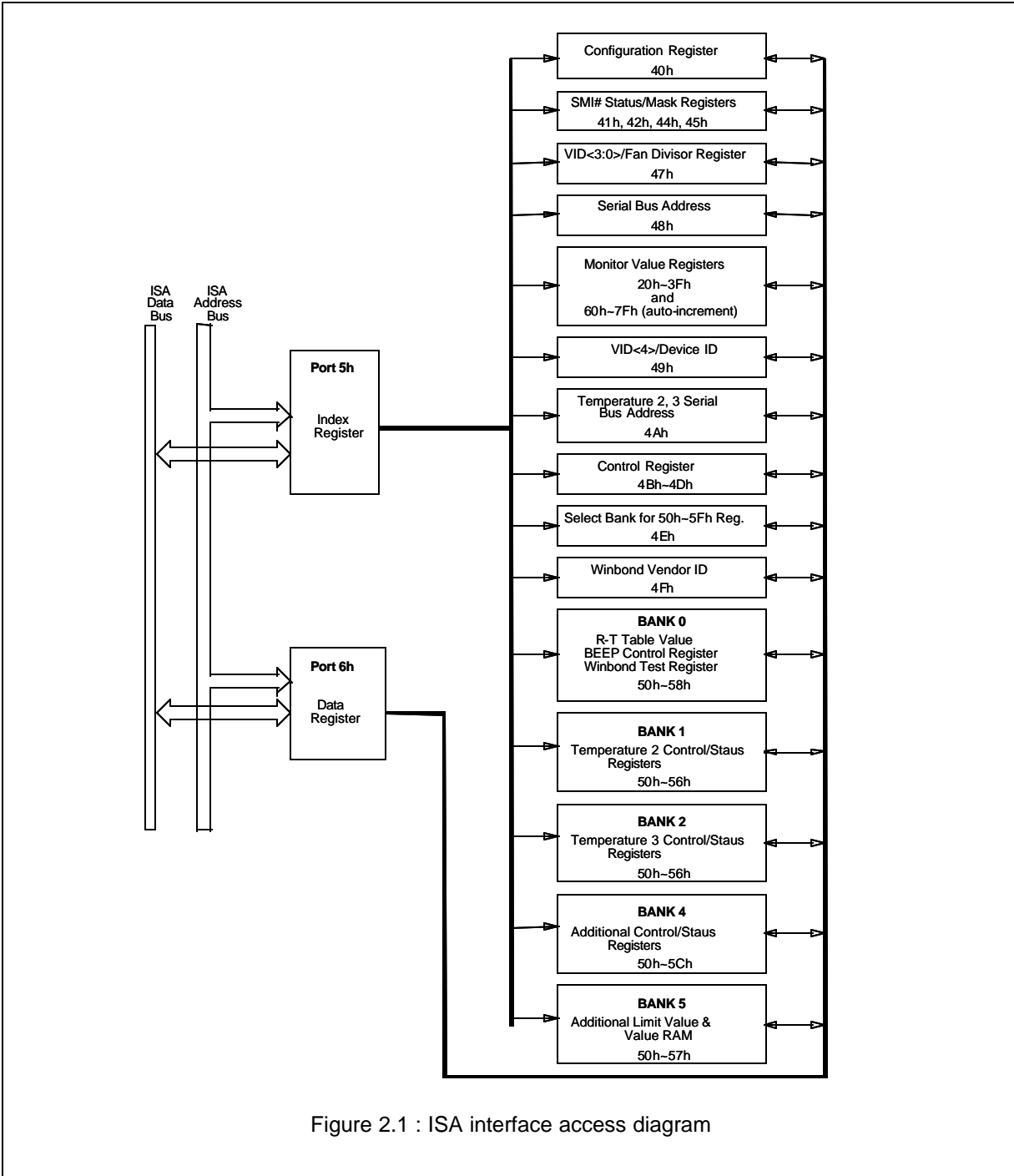The register structure is showed as the Figure 2.1

Figure 2.1 : ISA interface access diagram

## 2.2.2 I²C interface

The second interface uses I²C Serial Bus. W83627HF hardware monitor has three serial bus address. That is, the first address defined at CR[48h] can read/write all registers excluding Bank 1 and Bank 2 temperature sensor 2/3 registers. The second address defined at CR[4Ah] bit2-0 only read/write temperature sensor 2 registers, and the third address defined at CR[4Ah] bit6-4 only can access (read/write) temperature sensor 3 registers.

### 2.2.2.1 The first serial bus access timing is shown as follow:

*(a) Serial bus write to internal address register followed by the data byte*
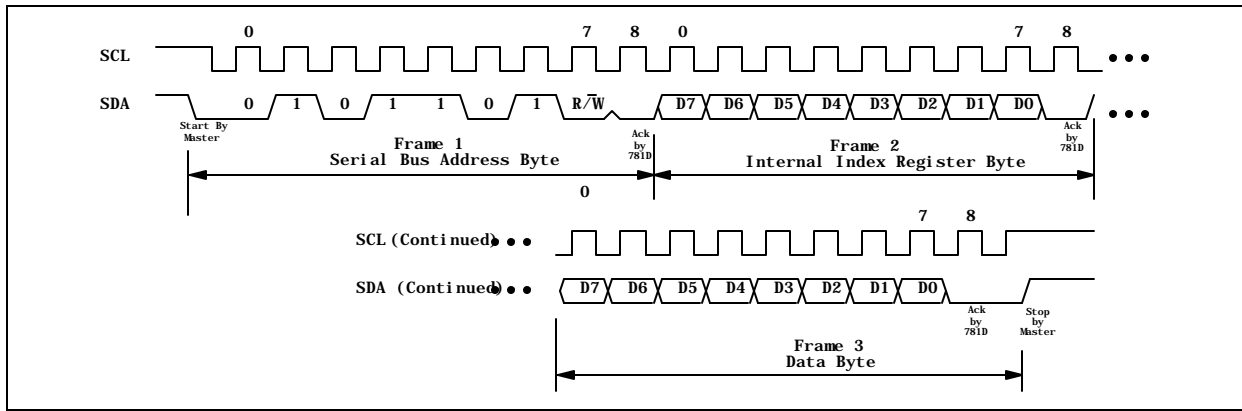


*(b) Serial bus write to internal address register only*
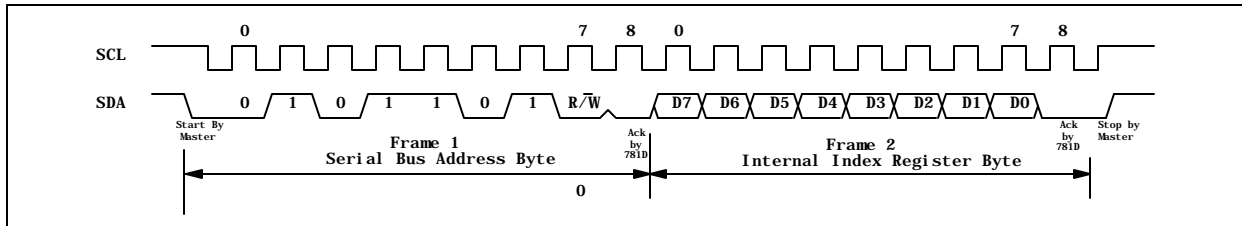


*(c) Serial bus read from a register with the internal address register prefer to desired location*
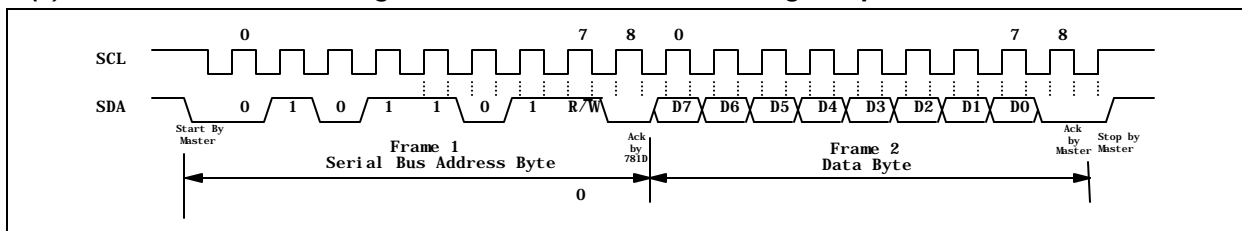


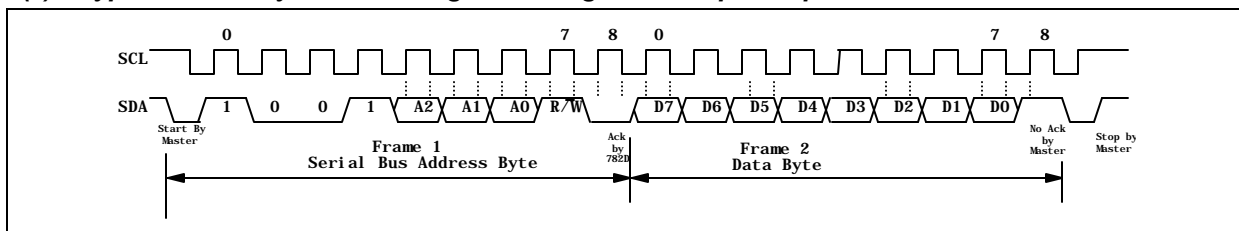### 2.2.2.2 The serial bus timing of the temperature 2 and 3 are shown as follow:

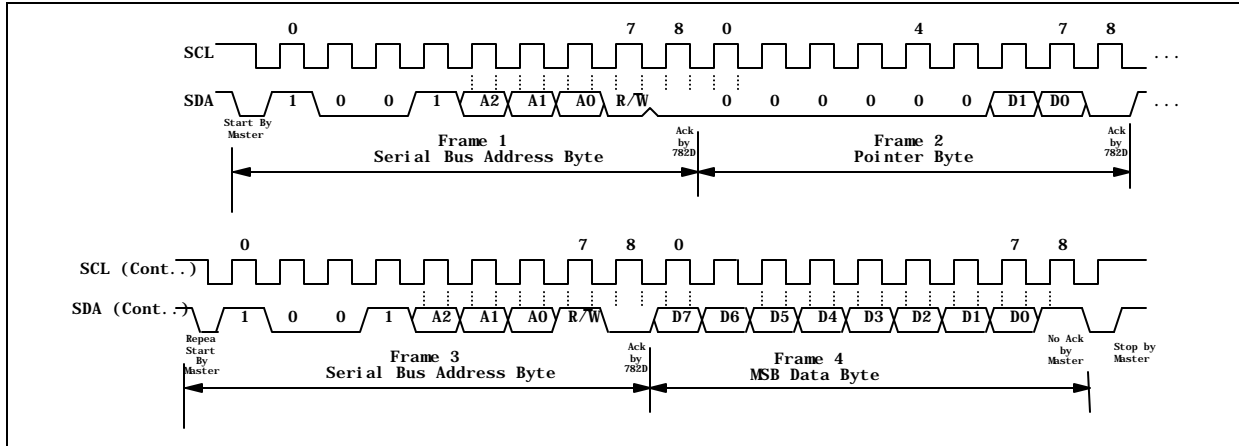**(a) Typical 2-byte read from preset pointer location (Temp, $T_{OS}$, $T_{HYST}$)**
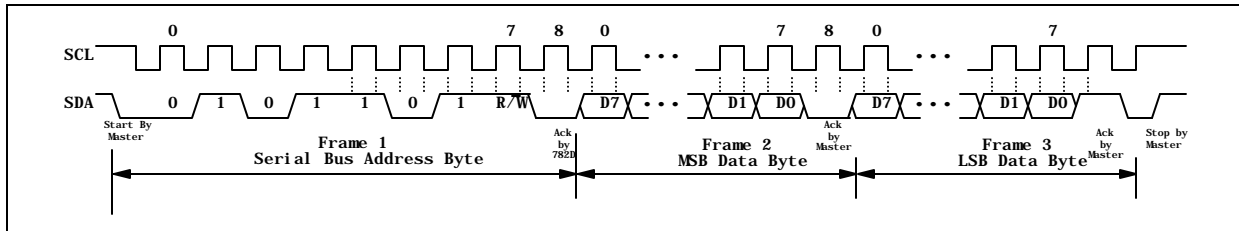
**(b)  Typical pointer set followed by immediate read for 2-byte register (Temp, $T_{OS}$, $T_{HYST}$)**
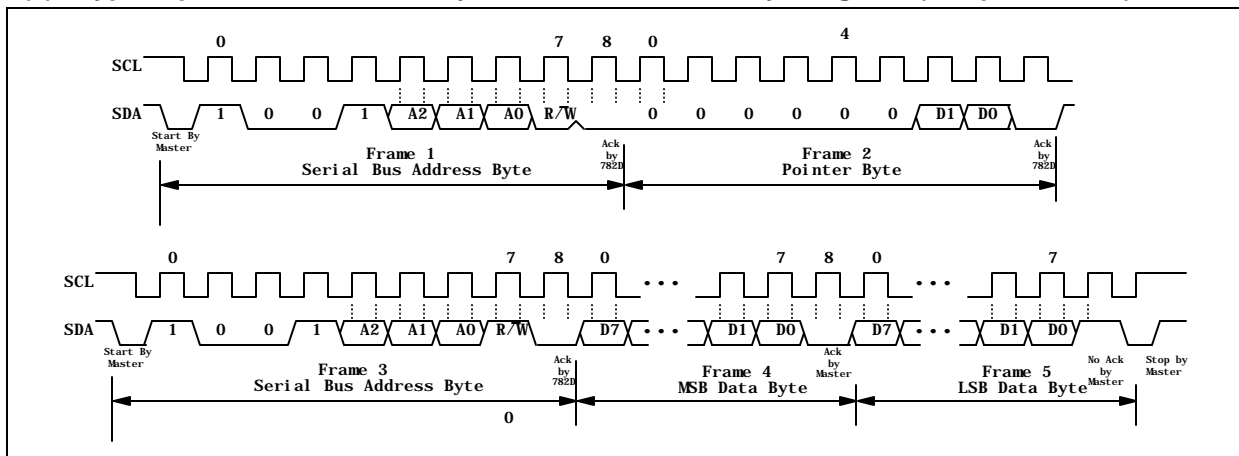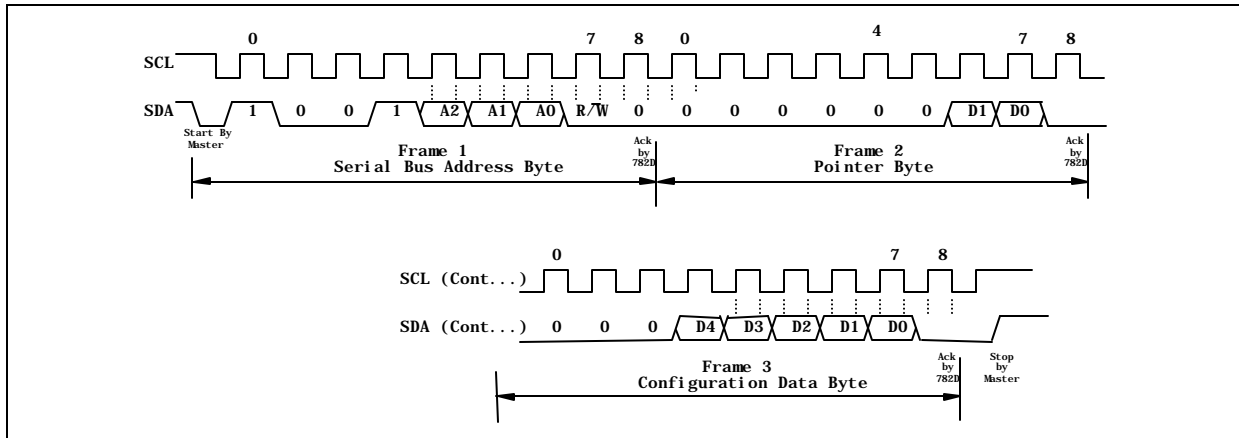


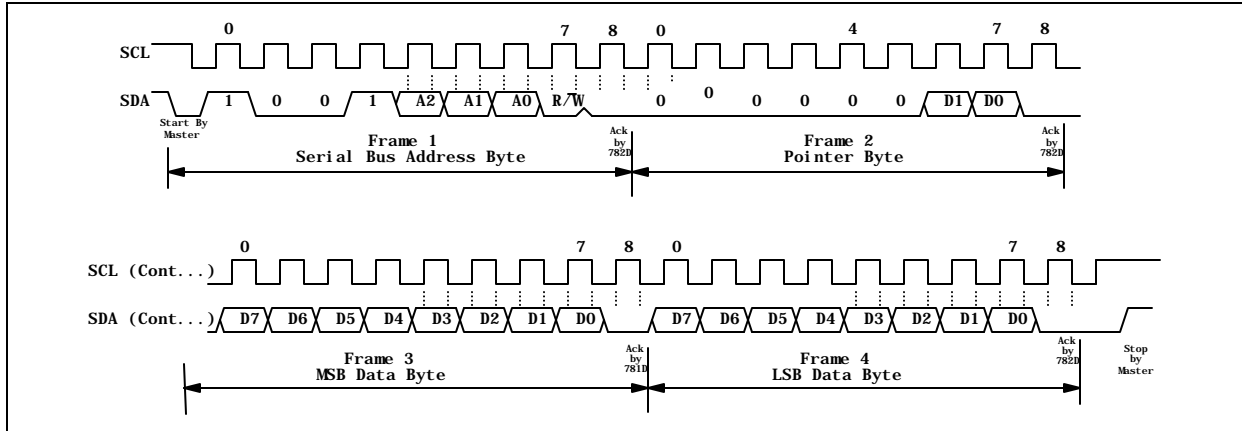*(c)  Typical read 1-byte from configuration register with preset pointer*

**(d)  Typical pointer set followed by immediate read from configuration register**



**(e) Temperature 2/3 configuration register Write**

**(f)** *Temperature 2/3 $T_{OS}$ and $T_{HYST}$ write*

## 2.3 Analog Inputs

The maximum input voltage of the analog pin is 4.096V because the 8-bit ADC has a 16mv LSB. Really, the application of the PC monitoring would most often be connected to power suppliers. The CPU V-core voltage ,+3.3V ,battery and 5VSB voltage can directly connected to these analog inputs. The +12V,-12V and -5V voltage inputs should be reduced a factor with external resistors so as to obtain the input range. As Figure 2.2 shows.
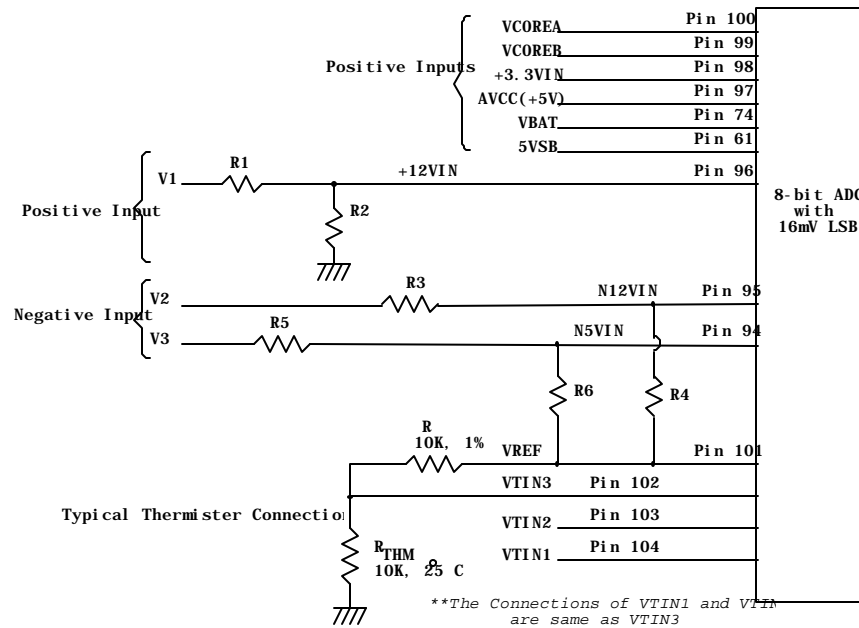


Figure. 2.2

### 2.3.1 Monitor over 4.096V voltage:

The input voltage +12VIN can be expressed as following equation.

$$12VIN = V_1 \times \frac{R_2}{R_1 + R_2}$$

The value of R1 and R2 can be selected to 28K Ohms and 10K Ohms, respectively, when the input voltage V1 is 12V. The node voltage of +12VIN can be subject to less than 4.096V for the maximun input range of the 8-bit ADC. The Pin 97 is connected to the power supply VCC with +5V. There are two functions in this pin with 5V. The first function is to supply internal analog power in the W83627HF and the second function is that this voltage with 5V  is connected to internal serial resistors to monitor the +5V voltage. The value of two serial resistors are 34K ohms and 50K ohms so that input voltage to ADC is 2.98V which is less than 4.096V of ADC maximum input voltage. The express equation can represent as follows.

$$V_{in} = VCC \times \frac{50K\Omega}{50K\Omega + 34K\Omega} \cong 2.98V$$

where VCC is set to 5V.

The Pin 61 is connected to 5VSB voltage. W83627HF monitors this voltage and the internal two serial resistors are 17K $\Omega$ and 33K $\Omega$ so that input voltage to ADC is 3.3V which less than 4.096V of ADC maximum input voltage.

### 2.3.2 Monitor negative voltage:

The negative voltage should be connected two series resistors and a positive voltage VREF (is equal to 3.6V). In the Figure 11.2, the voltage V2 and V3 are two negative voltage which they are -12V and -5V respectively. The voltage V2 is connected to two serial resistors then is connected to another terminal VREF which is positive voltage. So as that the voltage node N12VIN can be obtain a posedge voltage if the scales of the two serial resirtors are carefully selected. It is recommanded from Winbond that the scale of two serial resistors are R3=232K ohms and R4=56K ohm. The input voltage of node N12VIN can be calculated by following equation.

$$N12VIN = (VREF + |V_2|) \times (\frac{232K\Omega}{232K\Omega + 56K\Omega}) + V_2$$

where VREF is equal 3.6V.

If the V2 is equal to -12V then the voltage is equal to 0.567V and the converted hexdecimal data is set to 35h by the 8-bit ADC with 16mV-LSB.This monitored value should be converted to the real negative votage and the express equation is shown as follows.

$$V_2 = \frac{N12VIN - VREF \times \boldsymbol{b}}{1 - \boldsymbol{b}}$$

Where $\beta$ is 232K/(232K+56K). If the N2VIN is 0.567 then the V2 is approximately equal to -12V.

The another negative voltage input V3 (approximate -5V) also can be evaluated by the similar method and the serial resistors can be selected with R5=120K ohms and R6=56K ohms by the Winbond recommended. The expression equation of V3 With -5V voltage is shown as follows.

$$V_3 = \frac{N5VIN - VREF \times \boldsymbol{g}}{1 - \boldsymbol{g}}$$

Where the $\gamma$ is set to 120K/(120K+56K). If the monitored ADC value in the N5VIN channel is 0.8635,

VREF=3.6V and the parameter $\gamma$ is 0.6818 then the negative voltage of V3 can be evalated to be -5V.

### 2.3.3 Temperature Measurement Machine

The temperature data format is 8bit two's-complement for sensor 2 and 9bit two's-complement for sensor 1. The 8-bit temperature data can be obtained by reading the CR[27h]. The 9-bit temperature data can be obtained by reading the 8 MSBs from the Bank1 CR[50h] and the LSB from the Bank1 CR[51h] bit 7. The format of the temperature data is show in Table 1.

| Temperature | 8-Bit Digital Output | | 9-Bit Digital Output | |
|---|---|---|---|---|
| | 8-Bit Binary | 8-Bit Hex | 9-Bit Binary | 9-Bit Hex |
| +125°C | 0111,1101 | 7Dh | 0,1111,1010 | 0FAh |
| +25°C | 0001,1001 | 19h | 0,0011,0010 | 032h |
| +1°C | 0000,0001 | 01h | 0,0000,0010 | 002h |
| +0.5°C | - | - | 0,0000,0001 | 001h |
| +0°C | 0000,0000 | 00h | 0,0000,0000 | 000h |
| -0.5°C | - | - | 1,1111,1111 | 1FFh |
| -1°C | 1111,1111 | FFh | 1,1111,1110 | 1FFh |
| -25°C | 1110,0111 | E7h | 1,1100,1110 | 1CEh |
| -55°C | 1100,1001 | C9h | 1,1001,0010 | 192h |

**Table 2.**

### 2.3.3.1 Monitor temperature from thermistor:

The W83627HF can connect three thermistors to measure three different envirment temperature. The specification of thermistor should be considered to (1) β value is 3435K, (2) resistor value is 10K ohms at 25°C. In the Figure 2.2, the themistor is connected by a serial resistor with 10K Ohms, then connect to VREF (Pin 101).

### 2.3.3.2 Monitor temperature from Pentium II™ thermal diode or bipolar transistor 2N3904

The W83627HF can alternate the thermistor to Pentium II™ (Deschutes) thermal diode interface or transistor 2N3904 and the circuit connection is shown as Figure 2.3. The pin of Pentium II™ D- is connected to power supply ground (GND) and the pin D+ is connected to pin VTINx in the W83627HF. The resistor R=30K ohms should be connected to VREF to supply the diode bias current and the bypass capacitor C=3300pF should be added to filter the high frequency noise. The transistor 2N3904 should be connected to a form with a diode, that is, the Base (B) and Collector (C) in the 2N3904 should be tied togeter to act as a thermal diode.
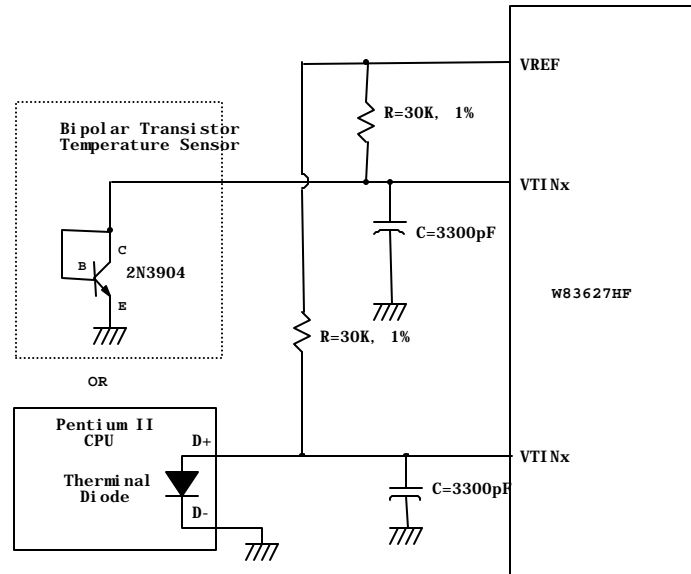
Figure 2.3

## 2.4 FAN Speed Count and FAN Speed Control

### 2.4.1 Fan speed count

Inputs are provides for signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage can not be over +5.5V. If the input signals from the tachometer outputs are over the VCC, the external trimming circuit should be added to reduce the voltage to obtain the input specification. The normal circuit and trimming circuits are shown as Figure 2.4.

Determine the fan counter according to:

$$Count = \frac{1.35 \times 10^6}{RPM \times Divisor}$$

In other words, the fan speed counter has been read from register CR28 or CR29 or CR2A, the fan speed can be evaluated by the following equation.

$$RPM = \frac{1.35 \times 10^6}{Count \times Divisor}$$

The default divisor is 2 and defined at CR47.bit7~4, CR4B.bit7~6, and Bank0 CR5D.bit5~7 which are three bits for divisor. That provides very low speed fan counter such as power supply fan. The followed table is an example for the relation of divisor, PRM, and count.

| Divisor | Nominal PRM | Time per Revolution | Counts | 70% RPM | Time for 70% |
|---|---|---|---|---|---|
| 1 | 8800 | 6.82 ms | *153* | 6160 | 9.74 ms |
| 2 (default) | 4400 | 13.64 ms | *153* | 3080 | 19.48 ms |
| 4 | 2200 | 27.27 ms | *153* | 1540 | 38.96 ms |
| 8 | 1100 | 54.54 ms | *153* | 770 | 77.92 ms |
| 16 | 550 | 109.08 ms | *153* | 385 | 155.84 ms |
| 32 | 275 | 218.16 ms | *153* | 192 | 311.68 ms |
| 64 | 137 | 436.32 ms | *153* | 96 | 623.36 ms |
| 128 | 68 | 872.64 ms | *153* | 48 | 1246.72 ms |

Table 1.
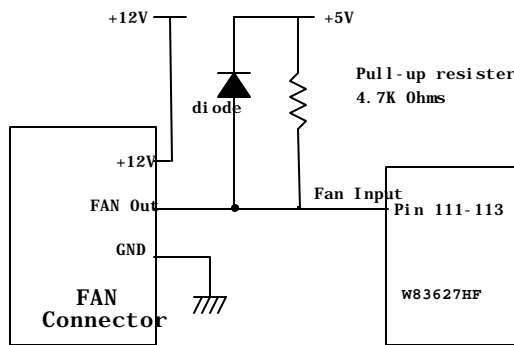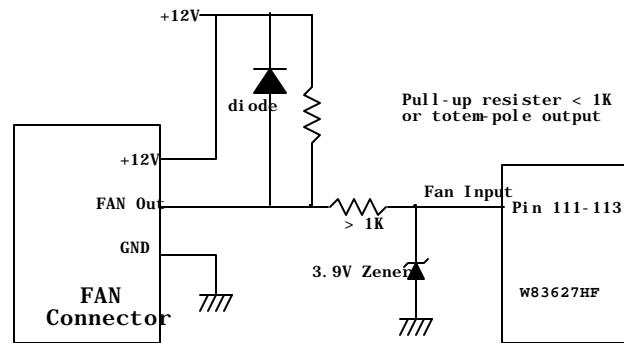
Fan with Tach Pull-Up to +5
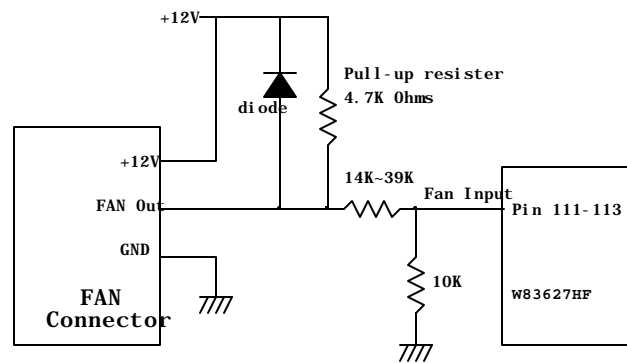
Fan with Tach Pull-Up to +12V, or Totem-Pole Output and Register Attenuator
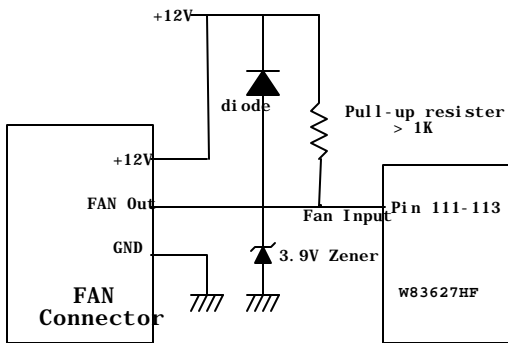
Fan with Tach Pull-Up to +12V and Zener

Fan with Tach Pull-Up to +12V, or Totem-Output and Zener Clamp

Figure 2.4

2.4.2 Fan speed control

The W83627HF provides 2 sets for fan PWM speed control. The duty cycle of PWM can be programmed by a 8-bit registers which are defined in the Bank0 CR5A and CR5B. The default duty cycle is set to 100%, that is, the default 8-bit registers is set to FFh. The expression of duty can be represented as follows.

$$\text{Duty} - \text{cycle}(\%) = \frac{\text{Programmed 8 - bit Register Value}}{255} \times 100\%$$

The PWM clock frequency also can be program and defined in the Bank0.CR5C . The application circuit is shown as follows.
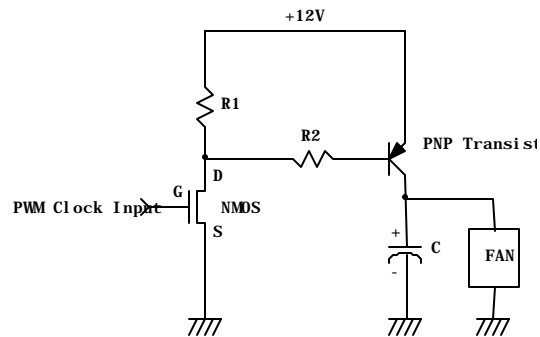


Figure 2.5

## 2.5 SMI# interrupt mode

### 2.5.1 Voltage SMI# mode :

SMI# interrupt for voltage is Two-Times Interrupt Mode. Voltage exceeding high limit or going below low limit will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 2.6 )

## 2.5.2 Fan SMI# mode :

SMI# interrupt for fan is Two-Times Interrupt Mode. Fan count exceeding the limit, or exceeding and then going below the limit, will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 2.7 )



*Interrupt Reset when Interrupt Status Registers are read

Figure 2.6                                          Figure 2.7

## 2.5.3 The W83627HF temperature sensor 1 SMI# interrupt has two modes:

**(1) Comparator Interrupt Mode**

Setting the $T_{HYST}$ (Temperature Hysteresis) limit to 127°C will set temperature sensor 1 SMI# to the Comparator Interrupt Mode. Temperature exceeds $T_O$ (Over Temperature) Limit causes an interrupt and this interrupt will be reset by reading all the Interrupt Status Register. Once an interrupt event has occurred by exceeding $T_O$, then reset, if the temperature remains above the $T_O$ , the interrupt will occur again when the next conversion has completed. If an interrupt event has occurred by exceeding $T_O$ and not reset, the interrupts will not occur again. The interrupts will continue to occur in this manner until the temperature goes below $T_O$. (Figure 2.8 )

![Winbond Electronics Corp. logo]

**W83627HF/F**

**(2) Two-Times Interrupt Mode**

Setting the $T_{HYST}$ lower than $T_O$ will set temperature sensor 1 SMI# to the Two-Times Interrupt Mode. Temperature exceeding $T_O$ causes an interrupt and then temperature going below $T_{HYST}$ will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once an i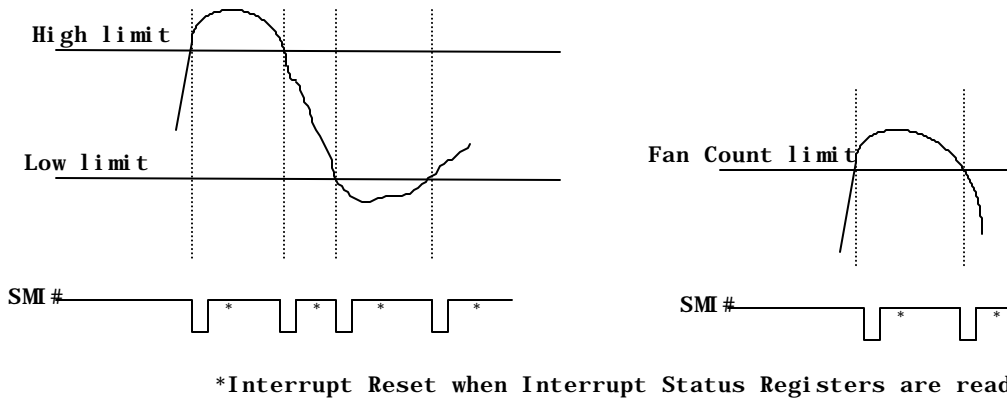nterrupt event has occurred by exceeding $T_O$ , then reset, if the temperature remains above the $T_{HYST}$ , the interrupt will not occur. (Figure 2.9 )



*Interrupt Reset when Interrupt Status Registers are read

Figure 2.8                                                              Figure 2.9

2.5.4 The W83627HF temperature sensor 2 and sensor 3 SMI# interrupt has two modes and it is programmed at CR[4Ch] bit 6.

**(1) Comparator Interrupt Mode**

Temperature exceeding $T_O$ causes an interrupt and this interrupt will be reset by reading all the Interrupt Status Register. Once an interrupt event has occurred by exceeding $T_O$, then reset, if the temperature remains above the $T_{HYST}$, the interrupt will occur again when the next conversion has completed. If an interrupt event has occurred by exceeding $T_O$ and not reset, the interrupts will not occur again. The interrupts will continue to occur in this manner until the temperature goes below $T_{HYST}$. ( Figure 2.10 )

**(2) Two-Times Interrupt Mode**

Temperature exceeding $T_O$ causes an interrupt and then temperature going below $T_{HYST}$ will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once an interrupt event has occurred by exceeding $T_O$, then reset, if the temperature remains above the $T_{HYST}$, the interrupt will not occur. (Figure 2.11 )
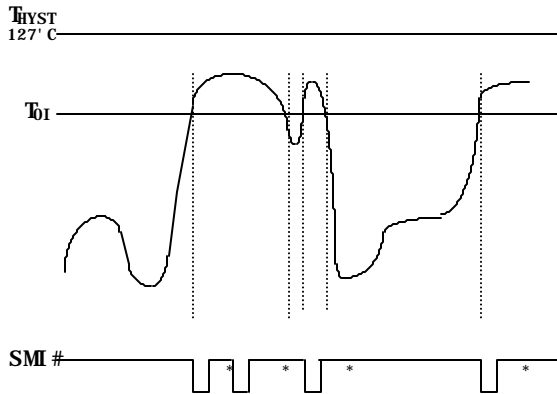
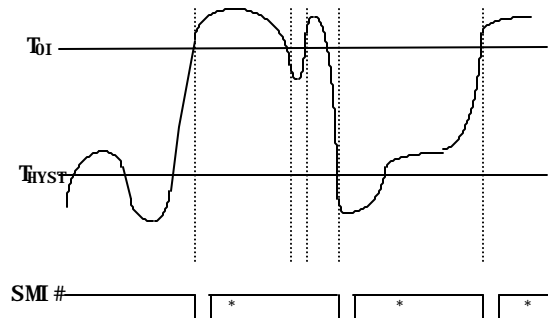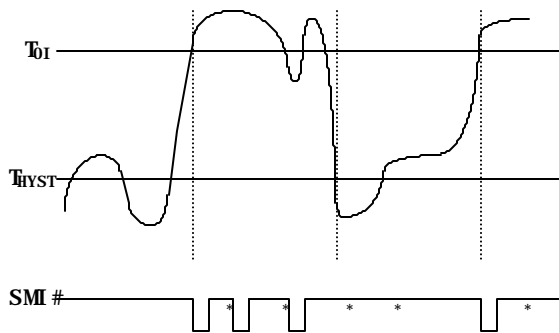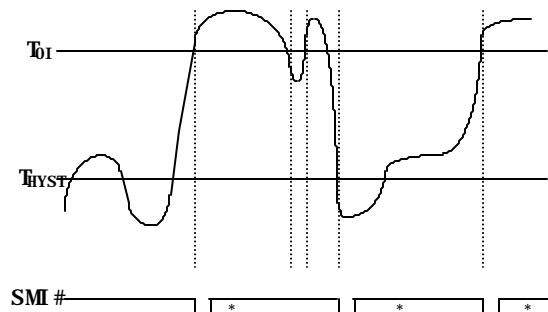*Interrupt Reset when Interrupt Status Registers are read

Figure 2.10                    Figure 2.11

### 2.6 OVT# interrupt mode

The OVT# signal is only related with temperature sensor 2 and 3 (VTIN2 / VTIN3).

### 2.6.1 The W83627HF temperature sensor 2 and 3 Over-Temperature (OVT#) has the following modes

**(1) Comparator Mode :**

Setting Bank1/2 CR[52h] bit 2 to 0 will set OVT# signal to comparator mode. Temperature exceeding $T_O$ causes the OVT# output activated until the temperature is less than $T_{HYST}$. ( Figure 2.12)

**(2) Interrupt Mode:**

Setting Bank1/2 CR[52h] bit 2 to 1 will set OVT# signal to interrupt mode. Setting Temperature exceeding $T_O$ causes the OVT# output activated indefinitely until reset by reading temperature sensor 2 or sensor 3 registers. Temperature exceeding $T_O$, then OVT# reset, and then temperature going below $T_{HYST}$ will also cause the OVT# activated indefinitely until reset by reading temperature sensor2 or sensor 3 registers. Once the OVT# is activated by exceeding $T_O$, then reset, if the temperature remains above $T_{HYST}$, the OVT# will not be activated again.( Figure 2.12)



*Interrupt Reset when Temperature 2/3 is read
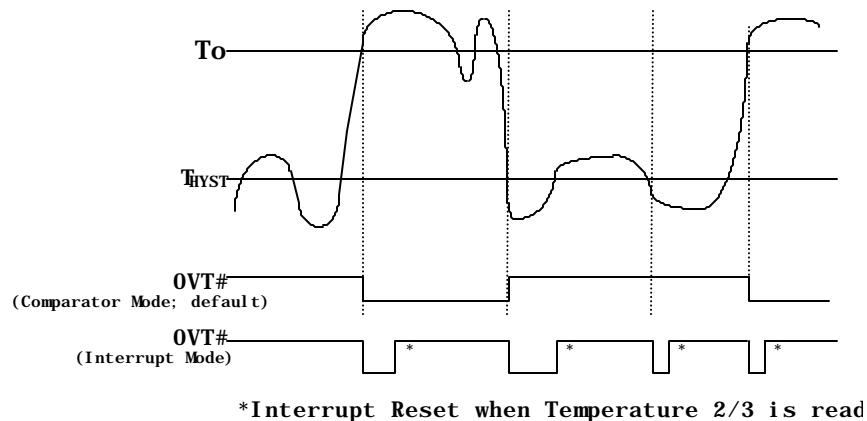
## 2.7 REGISTERS AND RAM

**Address Register (Port x5h)**

Data Port:                          Port x5h

Power on Default Value              00h

Attribute:                          Bit 6:0 Read/write , Bit 7: Read Only

Size:                               8 bits
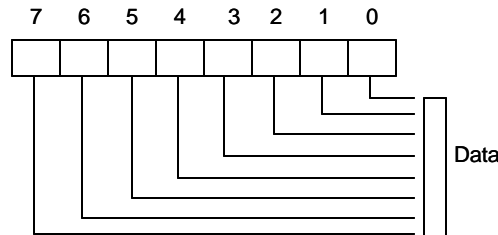


Bit7: Read Only

The logical 1 indicates the device is busy because of a Serial Bus transaction or another LPC bus transaction. With checking this bit, multiple LPC drivers can use W83627HF hardware monitor without interfering with each other or a Serial Bus driver.

It is the user's responsibility not to have a Serial Bus and LPC bus operations at the same time.

This bit is:

**Set:** with a write to Port x5h or when a Serial Bus transaction is in progress.

**Reset:** with a write or read from Port x6h if it is set by a write to Port x5h, or when the Serial Bus transaction is finished.

Bit 6-0: Read/Write

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Busy | Address Pointer (Power On default 00h) | | | | | | |
| (Power On default 0) | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

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**Address Pointer Index (A6-A0)**

| Registers and RAM | A6-A0 in Hex | Power On Value of Registers: <k7:0>in Binary | Notes |
|---|---|---|---|
| Configuration Register | 40h | 00001000 | |
| Interrupt Status Register 1 | 41h | 00000000 | Auto-increment to the address of Interrupt Status Register 2 after a read or write to Port x6h. |
| Interrupt Status Register 2 | 42h | 00000000 | |
| SMI#Ý Mask Register 1 | 43h | 00000000 | Auto-increment to the address of SMIÝ Mask Register 2 after a read or write to Port x6h. |
| SMIÝ Mask Register 2 | 44h | 00000000 | |
| NMI Mask Register 1 | 45h | 00000000 | Auto-increment to the address of NMI Mask Register 2 after a read or write to Port x6h |
| NMI Mask Register 2 | 46h | 01000000 | |
| VID/Fan Divisor Register | 47h | <7:4> = 0101; <3:0> = VID3-VID0 | |
| Serial Bus Address Register | 48h | <7> = 0 ; <6:0> = 0101101 | |
| VID4 & Device ID Register | 49h | <7:1> = 0000001; <0> = VID4 | |
| Temperature 2 and Temperature 3 Serial Bus Address Register | 4Ah | <7:0> = 00000001 | |
| Pin Control Register | 4Bh | <7:0> = 01000100 | |
| IRQ/OVT# Property Select Register | 4Ch | <7:0> = 00000000 | |
| FAN IN/OUT and BEEP Control Register | 4Dh | <7:0> = 00010101 | |
| Register 50h-5Fh Bank Select Register | 4Eh | <7> = 1 ; <6:3> = Reserved ; <2:0> = 000 | |

Address Pointer Index (A6-A0), continued

| Registers and RAM | A6-A0 in Hex | Power On Value of Registers: <k7:0>in Binary | NOTES |
|---|---|---|---|
| Winbond Vendor ID Register | 4Fh | <7:0> = 01011100 (High Byte)<br><7:0> = 10100011 (LOW BYTE) | |
| POST RAM | 00-1Fh | | Auto-increment to the next location after a read or write to Port x6h and stop at 1Fh. |
| Value RAM | 20-3Fh | | |
| Value RAM | 60-7Fh | | Auto-increment to the next location after a read or write to Port x6h and stop at 7Fh. |
| Temperature 2 Registers | Bank1<br>50h-56h | | |
| Temperature 3 Registers | Bank2<br>50h-56h | | |
| Additional Configuration Registers | Bank4<br>50h-5Dh | | |

**Data Register (Port x6h)**

Data Port:                          Port x6h

Power on Default Value              00h

Attribute:                          Read/write
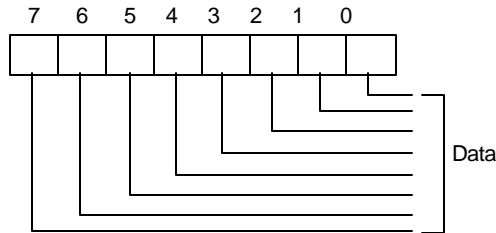
Size:                               8 bits



Bit 7-0: Data to be read from or to be written to RAM and Register.

**Configuration Register ¾ Index 40h**

Register Location:                  40h

Power on Default Value              01h

Attribute:                          Read/write

Size:                               8 bits
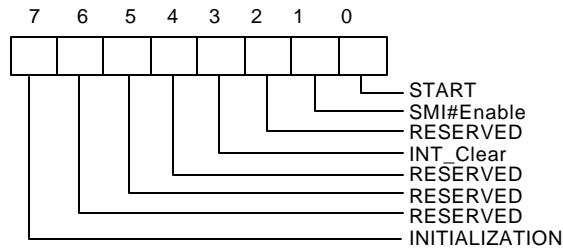


Bit 7: A one restores power on default value to all registers except the Serial Bus Address register.  This bit clears itself since the power on default is zero.

Bit 6: Reserced

Bit 5: Reserved

Bit 4: Reserved

Bit 3: A one disables the SMI# output without affecting the contents of Interrupt Status      Registers. The device will stop monitoring. It will resume upon clearing of this bit.

Bit 2: Reserved

Bit 1: A one enables the SMI# Interrupt output.

Bit 0: A one enables startup of monitoring operations, a zero puts the part in standby mode.

**Note:** The outputs of Interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred unlike "INT_Clear" bit.

**Interrupt Status Register 1¾ Index 41h**

Register Location:            41h

Power on Default Value      00h

Attribute:                  Read Only

Size:                       8 bits

```
 7   6   5   4   3   2   1   0
┌───┬───┬───┬───┬───┬───┬───┬───┐
└───┴───┴───┴───┴───┴───┴───┴───┘
                            └── VCOREA
                        └────── VCOREB
                    └────────── +3.3VIN
                └────────────── +5VIN
            └────────────────── TEMP1
        └────────────────────── TEMP2
    └────────────────────────── FAN1
└──────────────────────────────── FAN2
```
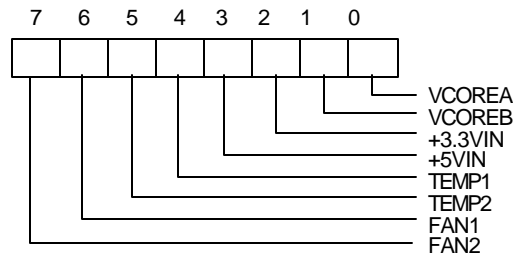
Bit 7: A one indicates the fan count limit of FAN2 has been exceeded.

Bit 6: A one indicates the fan count limit of FAN1 has been exceeded.

Bit 5: A one indicates a High limit of VTIN2 has been exceeded from temperature sensor 2.

Bit 4: A one indicates a High limit of VTIN1 has been exceeded from temperature sensor 1.

Bit 3: A one indicates a High or Low limit of +5VIN has been exceeded.

Bit 2: A one indicates a High or Low limit of +3.3VIN has been exceeded.

Bit 1: A one indicates a High or Low limit of VCOREB has been exceeded.

Bit 0: A one indicates a High or Low limit of VCOREA has been exceeded.

**Interrupt Status Register 2 ¾ Index 42h**

| | |
|---|---|
| Register Location: | 42h |
| Power on Default Value | 00h |
| Attribute: | Read Only |
| Size: | 8 bits |

```
        7   6   5   4   3   2   1   0
      ┌───┬───┬───┬───┬───┬───┬───┬───┐
      │   │   │   │   │   │   │   │   │
      └───┴───┴───┴───┴───┴───┴───┴───┘
                                    └── +12VIN
                                └────── -12VIN
                            └────────── -5VIN
                        └────────────── FAN3
                    └────────────────── Chassis Intrusion
                └────────────────────── Temp3
            └────────────────────────── Reserved
        └────────────────────────────── Reserved
```

Bit 7-6:Reserved.This bit should be set to 0.

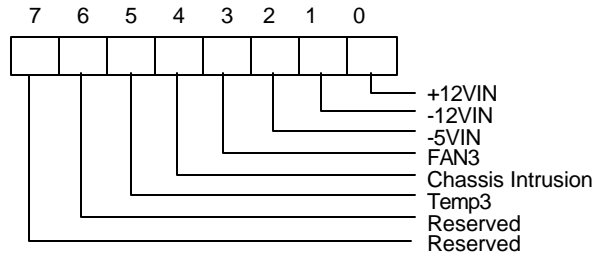Bit 5: A one indicates a High limit of VTIN3 has been exceeded  from temperature sensor 3.

Bit 4: A one indicates Chassis Intrusion has gone high.

Bit 3: A one indicates the fan count limit of FAN3 has been exceeded.

Bit 2: A one indicates a High or Low limit of -5VIN has been exceeded.

Bit1: A one indicates a High or Low limit of -12VIN has been exceeded.

Bit0: A one indicates a High or Low limit of +12VIN has been exceeded.


**SMI# Mask Register 1 ¾ Index 43h**

| | |
|---|---|
| Register Location: | 43h |
| Power on Default Value | 00h |
| Attribute: | Read/Write |
| Size: | 8 bits |

```
        7   6   5   4   3   2   1   0
      ┌───┬───┬───┬───┬───┬───┬───┬───┐
      │   │   │   │   │   │   │   │   │
      └───┴───┴───┴───┴───┴───┴───┴───┘
                                    └── VCOREA
                                └────── VCOREB
                            └────────── +3.3VIN
                        └────────────── +5VIN
                    └────────────────── TEMP1
                └────────────────────── TEMP2
            └────────────────────────── FAN1
        └────────────────────────────── FAN2
```
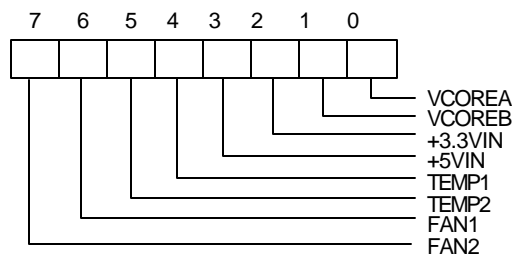
Bit 7-0: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

**SMI# Mask Register 2 ¾ Index 44h**

Register Location:                44h

Power on Default Value        00h

Attribute:                            Read/Write

Size:                                  8 bits

```
    7   6   5   4   3   2   1   0
  ┌───┬───┬───┬───┬───┬───┬───┬───┐
  │   │   │   │   │   │   │   │   │
  └───┴───┴───┴───┴───┴───┴───┴───┘
                              └── +12VIN
                          └────── -12VIN
                      └────────── -5VIN
                  └────────────── FAN3
              └────────────────── Chassis Intrusion
          └────────────────────── TEMP3
      └────────────────────────── Reserved
  └────────────────────────────── Reserved
```

Bit 7-6: Reserved. This bit should be set to 0.

Bit 5-0: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.


**Reserved Register ¾ Index 45h**


Chassis Clear Register -- Index 46h
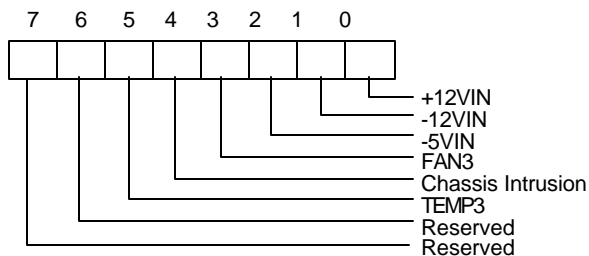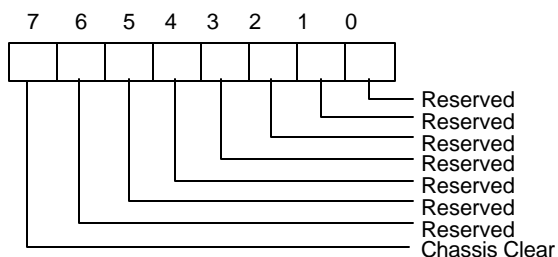
Register Location:                46h

Power on Default Value        00h

Attribute:                            Read/Write

Size:                                  8 bits

```
    7   6   5   4   3   2   1   0
  ┌───┬───┬───┬───┬───┬───┬───┬───┐
  │   │   │   │   │   │   │   │   │
  └───┴───┴───┴───┴───┴───┴───┴───┘
                              └── Reserved
                          └────── Reserved
                      └────────── Reserved
                  └────────────── Reserved
              └────────────────── Reserved
          └────────────────────── Reserved
      └────────────────────────── Reserved
  └────────────────────────────── Chassis Clear
```

Bit 7: Set 1 , clear Chassis Intrusion event.  This bit self clears after clearing Chassis Intrusion event.

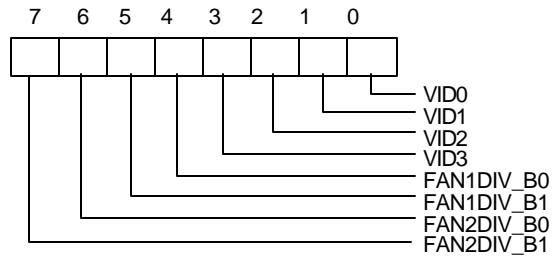Bit 6-0:Reserved. This bit should be set to 0.

**VID/Fan Divisor Register ¾ Index 47h**

Register Location:          47h

Power on Default Value  <7:4> is 0101, <3:0> is mapped to VID<3:0>

Attribute:                  Read/Write

Size:                       8 bits

```
         7   6   5   4   3   2   1   0
       ┌───┬───┬───┬───┬───┬───┬───┬───┐
       └───┴───┴───┴───┴───┴───┴───┴───┘
                                    └──── VID0
                                └──────── VID1
                            └──────────── VID2
                        └──────────────── VID3
                    └──────────────────── FAN1DIV_B0
                └──────────────────────── FAN1DIV_B1
            └──────────────────────────── FAN2DIV_B0
        └──────────────────────────────── FAN2DIV_B1
```

Bit 7-6: FAN2 Speed Control.

Bit 5-4: FAN1 Speed Control.

Bit 3-0: The VID <3:0> inputs
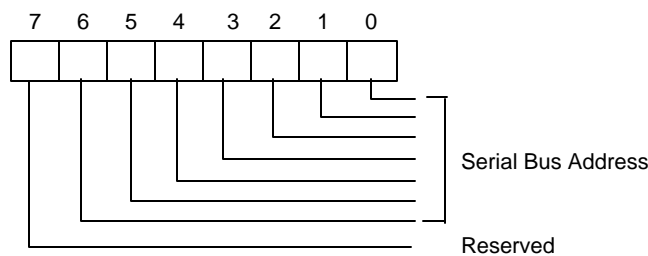
Note :  Please refer to Bank0 CR[5Dh] , Fan divisor table.

**Serial Bus Address Register ¾ Index 48h**

Register Location:                        48h

Power on Default Value  Serial Bus address        2Dh

Size:                                     8 bits

```
         7   6   5   4   3   2   1   0
       ┌───┬───┬───┬───┬───┬───┬───┬───┐
       └───┴───┴───┴───┴───┴───┴───┴───┘
                                    └────┐
                                └────────┤
                            └────────────┤
                        └────────────────┤── Serial Bus Address
                    └────────────────────┤
                └────────────────────────┤
            └────────────────────────────┘
        └──────────────────────────────────── Reserved
```

Bit 7: Read Only  - Reserved.

Bit 6-0: Read/Write  - Serial Bus address <6:0>.

**Value RAM ¾ Index 20h- 3Fh or 60h - 7Fh (auto-increment)**

| Address A6-A0 | Address A6-A0 with Auto-Increment | Description |
|---|---|---|
| 20h | 60h | VCOREA reading |
| 21h | 61h | VCOREB reading |
| 22h | 62h | +3.3VIN reading |
| 23h | 63h | +5VIN reading |
| 24h | 64h | +12VIN reading |
| 25h | 65h | -12VIN reading |
| 26h | 66h | -5VIN reading |
| 27h | 67h | Temperature reading |
| 28h | 68h | FAN1 reading<br>**Note:** This location stores the number of counts of the internal clock per revolution. |
| 29h | 69h | FAN2 reading<br>**Note:** This location stores the number of counts of the internal clock per revolution. |
| 2Ah | 6Ah | FAN3 reading<br>**Note:** This location stores the number of counts of the internal clock per revolution. |
| 2Bh | 6Bh | VCOREA High Limit, default value is defined by Vcore Voltage +0.2v. |
| 2Ch | 6Ch | VCOREA Low Limit, default value is defined by Vcore Voltage -0.2v. |
| 2Dh | 6Dh | VCOREB High Limit. |
| 2Eh | 6Eh | VCOREB Low Limit. |
| 2Fh | 6Fh | +3.3VIN High Limit |
| 30h | 70h | +3.3VIN Low Limit |
| 31h | 71h | +5VIN High Limit |
| 32h | 72h | +5VIN Low Limit |
| 33h | 73h | +12VIN High Limit |
| 34h | 74h | +12VIN Low Limit |

**Value RAM ¾ Index 20h- 3Fh or 60h - 7Fh (auto-increment), continued**

| Address A6-A0 | Address A6-A0 with Auto-Increment | Description |
|---|---|---|
| 35h | 75h | -12VIN High Limit |
| 36h | 76h | -12VIN Low Limit |
| 37h | 77h | -5VIN High Limit |
| 38h | 78h | -5VIN Low Limit |
| 39h | 79h | Temperature sensor 1 (VTIN1) High Limit |
| 3Ah | 7Ah | Temperature sensor 1 (VTIN1)  Hysteresis Limit |
| 3Bh | 7Bh | FAN1 Fan Count Limit<br><br>**Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed. |
| 3Ch | 7Ch | FAN2 Fan Count Limit<br><br>**Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed. |
| 3Dh | 7Dh | FAN3 Fan Count Limit<br><br>**Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed. |
| 3E- 3Fh | 7E- 7Fh | Reserved |

Setting all  ones to the high limits for voltages and fans (0111 1111 binary for temperature) means interrupts will never be generated except the case when voltages go below the low limits.


**Voltage ID (VID4) & Device ID Register - Index 49h**

Register Location:                 49h
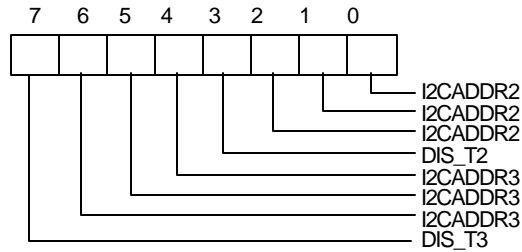
Power on Default Value        <7:1> is 000,0001 binary

<0> is mapped to VID <4>

Size:                                    8 bits
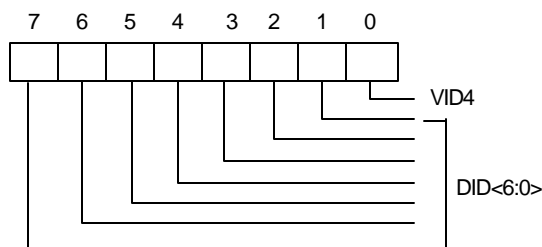


Bit 7-1: Read Only  - Device ID<6:0>

Bit 0 : Read/Write  - The VID4 inputs.

**Temperature 2 and Temperature 3 Serial Bus Address Register--Index 4Ah**

Register Location:          4Ah

Power on Default Value      01h

Attribute:                  Read/Write

Size:                       8 bits



Bit 7: Set to 1, disable temperature  sensor  3 and can not access any data from Temperature Sensor 3.

Bit 6-4: Temperature 3 Serial Bus Address. The serial bus address is 1001xxx. Where xxx are defined in these bits.

Bit 3: Set to 1, disable temperature Sensor 2 and can not access any data from Temperature Sensor 2.

Bit 2-0: Temperature 2 Serial Bus Address. The serial bus address is 1001xxx. Where xxx are defined in these bits.

**Pin Control Register - Index 4Bh**

Register Location:           4Bh

Power on Default Value       44h

Attribute:                   Read/Write

Size:                        8 bits
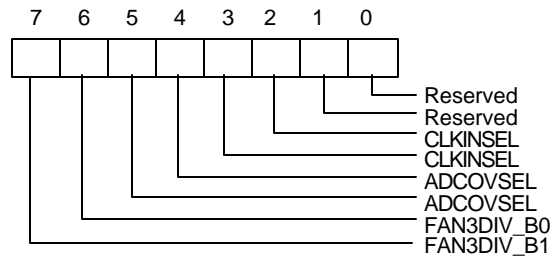


Bit 7-6: Fan3 speed divisor.

       Please refer to Bank0 CR[5Dh] , Fan divisor table.

Bit 5-4: Select A/D Converter Clock Input.

<5:4> = 00 - default. ADC clock select 22.5 Khz.

<5:4> = 01- ADC clock select 5.6 Khz. (22.5K/4)

<5:4> = 10 - ADC clock select 1.4Khz. (22.5K/16)

<5:4> = 11 - ADC clock select 0.35 Khz. (22.5K/64)

Bit 3-2: Clock Input Select.

<3:2> = 00 - Pin 3 (CLKIN) select 14.318M Hz clock.

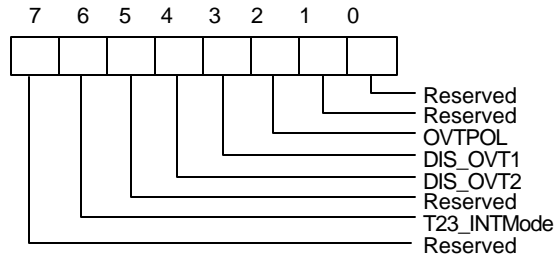<3:2> = 01 - Default. Pin 3 (CLKIN) select 24M Hz clock.

<3:2> = 10 - Pin 3 (CLKIN) select 48M Hz clock .

<3:2> = 11 - Reserved. Pin3 no clock input.

Bit 1-0: Reserved. User defined.

**IRQ/OVT# Property Select Register- Index 4Ch**

Register Location:                    4Ch

Power on Default Value                00h

Attribute:                            Read/Write

Size:                                 8 bits

```
      7   6   5   4   3   2   1   0
    ┌───┬───┬───┬───┬───┬───┬───┬───┐
    │   │   │   │   │   │   │   │   │
    └───┴───┴───┴───┴───┴───┴───┴───┘
                              └──────── Reserved
                          └──────────── Reserved
                      └──────────────── OVTPOL
                  └────────────────── DIS_OVT1
              └────────────────────── DIS_OVT2
          └────────────────────────── Reserved
      └────────────────────────────── T23_INTMode
    └────────────────────────────────── Reserved
```

Bit 7: Reserved. User Defined.

Bit6: Set to 1,  the SMI# output type of Temperature 2 and 3 is set to Comparator Interrupt  mode. Set to 0, the SMI# output type is set to Two-Times Interrupt mode. (default 0)

Bit5: Reserved. User Defined.

Bit 4: Disable temperature sensor 3 over-temperature (OVT) output if set to 1. Default 0, enable OVT2 output through pin OVT#.

Bit 3: Disable temperature sensor 2 over-temperature (OVT) output if set to 1. Default 0, enable OVT1 output through pin OVT#.
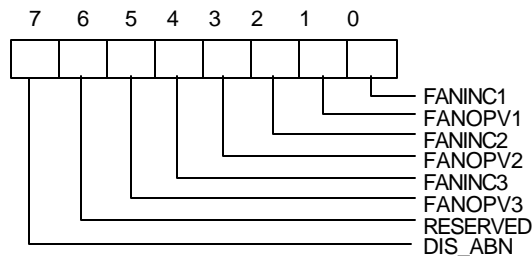
Bit 2: Over-temperature polarity. Write 1, OVT# active high. Write 0, OVT# active low. Default 0.

Bit 1: Reserved.

Bit 0: Reserved.

**FAN IN/OUT and BEEP Control Register- Index 4Dh**

Register Location:          4Dh

Power on Default Value      15h

Attribute:                  Read/Write

Size:                       8 bits

```
  7   6   5   4   3   2   1   0
┌───┬───┬───┬───┬───┬───┬───┬───┐
└───┴───┴───┴───┴───┴───┴───┴───┘
                            └── FANINC1
                        └────── FANOPV1
                    └────────── FANINC2
                └────────────── FANOPV2
            └────────────────── FANINC3
        └────────────────────── FANOPV3
    └────────────────────────── RESERVED
└────────────────────────────── DIS_ABN
```

Bit 7: Disable power-on abnormal the monitor voltage including V-Core A and +3.3V. If these voltage exceed the limit value, the pin (Open Drain) of BEEP will drives 300Hz and 600Hz frequency signal. Write 1, the frequency will be disable.  Default 0. After power on, the system should set     1  to this bit to 1 in order to disable BEEP.

Bit 6: Reserved.

Bit 5: FAN 3 output value if FANINC3 sets to 0. Write 1, then pin 18 always generate logic high signal. Write 0, pin 18 always generates logic low signal. This bit default 0.

Bit 4: FAN 3 Input Control. Set to 1, pin 18 acts as FAN clock input, which is default value. Set to 0, this pin 18 acts as FAN control signal and the output value of FAN control is set by this register     bit 5.

Bit 3: FAN 2 output value if FANINC2 sets to 0. Write 1, then pin 19 always generate logic high signal. Write 0, pin 19 always generates logic low signal. This bit default 0.

Bit 2: FAN 2 Input Control. Set to 1, pin 19 acts as FAN clock input, which is default value. Set to 0, this pin 19 acts as FAN control signal and the output value of FAN control is set by this register     bit 3.

Bit 1: FAN 1 output value if FANINC1 sets to 0. Write 1, then pin 20 always generate logic high signal. Write 0, pin 20 always generates logic low signal. This bit default 0.

Bit 0: FAN 1 Input Control. Set to 1, pin 20 acts as FAN clock input, which is default value. Set to 0, this pin 20 acts as FAN control signal and the output value of FAN control is set by this register     bit 1.

**Register 50h ~ 5Fh Bank Select Register - Index 4Eh (No Auto Increase)**
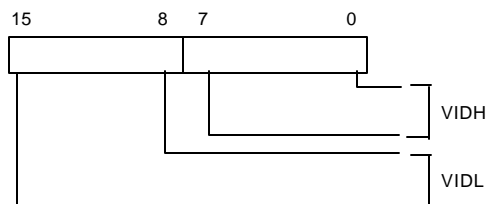
Register Location:        4Eh

Power on Default Value        80h

Attribute:        Read/Write

Size:        8 bits
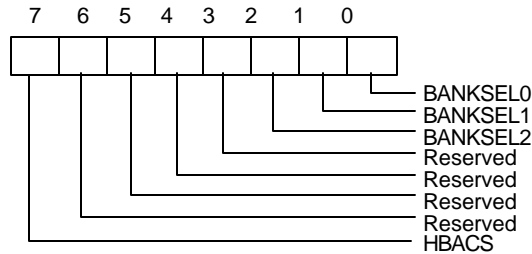


Bit 7: HBACS - High byte access. Set to 1, access Register 4Fh high byte register.

Set to 0, access Register 4Fh low byte register. Default 1.

Bit 6-3: Reserved. This bit should be set to 0.

Bit 2-0: Index ports 0x50~0x5F Bank select.


**Winbond Vendor ID Register - Index 4Fh (No Auto Increase)**

Register Location:        4Fh

Power on Default Value        <15:0> = 5CA3h

Attribute:        Read Only
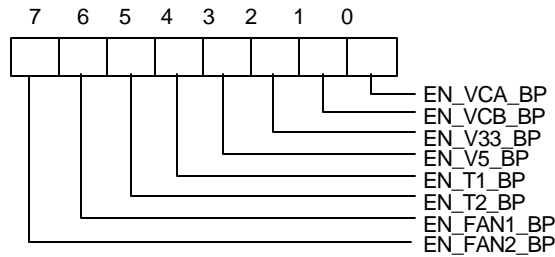
Size:        16 bits



Bit 15-8: Vendor ID High Byte if CR4E.bit7=1.Default 5Ch.

Bit 7-0: Vendor ID Low Byte if CR4E.bit7=0. Default A3h.

**Winbond Test  Register -- Index 50h - 55h (Bank 0)**

**BEEP Control Register 1-- Index 56h (*Bank 0*)**

| | |
|---|---|
| Register Location: | 56h |
| Power on Default Value | 00h |
| Attribute: | Read/Write |
| Size: | 8 bits |

```
       7   6   5   4   3   2   1   0
     ┌───┬───┬───┬───┬───┬───┬───┬───┐
     │   │   │   │   │   │   │   │   │
     └───┴───┴───┴───┴───┴───┴───┴───┘
                                 └──── EN_VCA_BP
                             └──────── EN_VCB_BP
                         └──────────── EN_V33_BP
                     └──────────────── EN_V5_BP
                 └──────────────────── EN_T1_BP
             └──────────────────────── EN_T2_BP
         └──────────────────────────── EN_FAN1_BP
     └──────────────────────────────── EN_FAN2_BP
```

Bit 7: Enable BEEP Output from FAN 2 if the monitor value exceed the limit value. Write 1, enable BEEP output, which is default value.

Bit 6: Enable BEEP Output from FAN 1 if the monitor value exceed the limit value. Write 1, enable BEEP output, which is default value.

Bit 5: Enable BEEP Output from Temperature Sensor 2 if the monitor value exceed the limit value. Write 1, enable BEEP output. Default 0

Bit 4: Enable BEEP output for Temperature Sensor 1 if the monitor value exceed the limit value. Write 1, enable BEEP output. Default 0

Bit 3: Enable BEEP output from VDD (+5V), Write 1, enable BEEP output if the monitor value exceed the limits value. Default 0, that is disable BEEP output.

Bit 2: Enable BEEP output from +3.3V. Write 1, enable BEEP output, which is default value.

Bit 1: Enable BEEP output from VCOREB. Write 1, enable BEEP output, which is default value.

Bit 0: Enable BEEP Output from VCOREA if the monitor value exceed the limits value. Write 1, enable BEEP output, which is default value
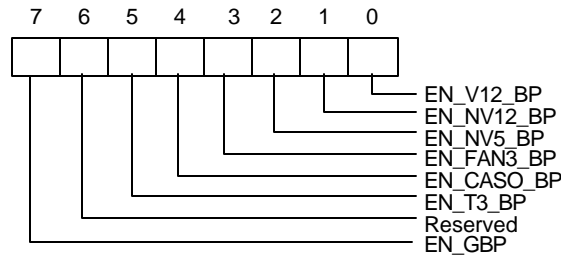
**BEEP Control Register 2-- Index 57h (*Bank 0*)**

Register Location:      57h

Power on Default Value  80h

Attribute:              Read/Write

Size:                   8 bits

```
      7   6   5   4   3   2   1   0
    ┌───┬───┬───┬───┬───┬───┬───┬───┐
    │   │   │   │   │   │   │   │   │
    └───┴───┴───┴───┴───┴───┴───┴───┘
                                  └── EN_V12_BP
                              └────── EN_NV12_BP
                          └────────── EN_NV5_BP
                      └────────────── EN_FAN3_BP
                  └────────────────── EN_CASO_BP
              └────────────────────── EN_T3_BP
          └────────────────────────── Reserved
      └────────────────────────────── EN_GBP
```

Bit 7: Enable Global BEEP. Write 1, enable global BEEP output. Default 1. Write 0, disable all BEEP output.

Bit 6: Reserved. This bit should be set to 0.

Bit5: Enable BEEP Output from Temperature Sensor 3 if the monitor value exceed the limit value. Write 1, enable BEEP output. Default 0

Bit 4: Enable BEEP output for case open if the monitor value exceed the limit value. Write 1, enable BEEP output. Default 0.

Bit 3: Enable BEEP Output from FAN 3 if the monitor value exceed the limit value. Write 1, enable BEEP output. Default 0.

Bit 2: Enable BEEP output from  -5V, Write 1, enable BEEP output if the monitor value exceed the limits value. Default 0, that is disable BEEP output.

Bit 1: Enable BEEP output from -12V, Write 1, enable BEEP output if the monitor value exceed the limits value. Default 0, that is disable BEEP output.

Bit 0: Enable BEEP output from +12V, Write 1, enable BEEP output if the monitor value exceed the limits value. Default 0, that is disable BEEP output.

**Chip ID -- Index 58h (*Bank 0*)**

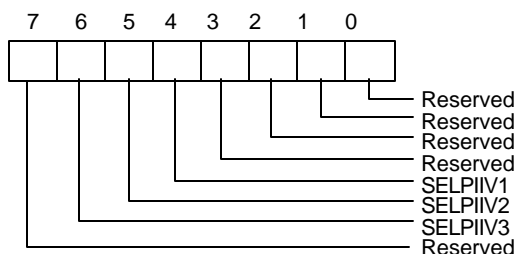Register Location:                  58h

Power on Default Value              21h

Attribute:                          Read Only
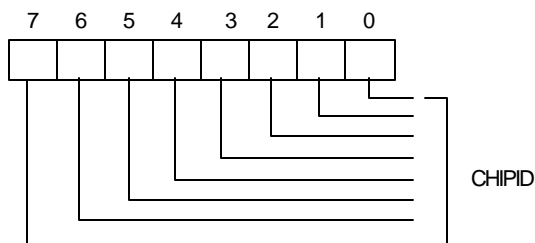
Size:                               8 bits



Bit 7: Winbond Chip ID number. Read this register will return 21h.

**Reserved Register  -- Index 59h (*Bank 0*)**

Register Location:                  59h

Power on Default Value              <7>=0 and <6:4> = 111 and <3:0> = 0000

Attribute:                          Read/Write

Size:                               8 bits



Bit 7: Reserved

Bit 6: Temperature sensor diode 3. Set to 1, select Pentium II compatible Diode. Set to 0 to select 2N3904 Bipolar mode.

Bit 5: Temperature sensor diode 2. Set to 1, select Pentium II compatible Diode. Set to 0 to select 2N3904 Bipolar mode.

Bit 4: Temperature sensor diode 1. Set to 1, select Pentium II compatible Diode. Set to 0 to select 2N3904 Bipolar mode.

Bit 3-0: Reserved

**PWMOUT1 Control -- Index 5Ah (*Bank 0*)**

Register Location:          5Ah

Power on default value:     FFh

Attribute:                  Read/Write

Size:                       8 bits

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

PWM1_DUTY
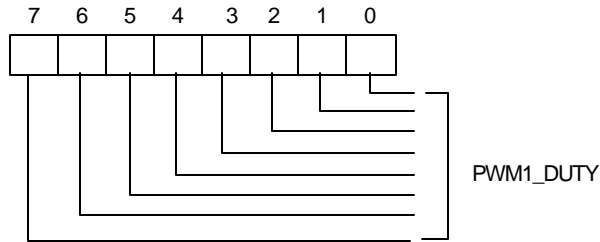
Bit 7: PWMOUT1 duty cycle control

Write FF, Duty cycle is 100%, Write 00, Duty cycle is 0%.
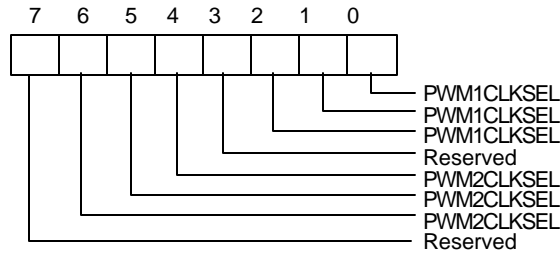
**PWMOUT2 Control -- Index 5Bh (*Bank 0*)**

Register Location:          5Bh

Power on default value:     FFh

Attribute:                  Read/Write

Size:                       8 bits

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |

PWM2_DUTY
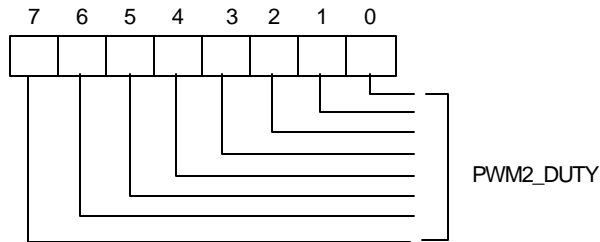
Bit 7: PWMOUT2 duty cycle control

Write FF, Duty cycle is 100%,    Write 00, Duty cycle is 0%.

**PWMOUT1/2 Clock Select -- Index 5Ch (*Bank 0*)**

Register Location:           5Ch

Power on Default Value       11h

Attribute:                   Read/Write

Size:                        8 bits

```
    7   6   5   4   3   2   1   0
  ┌───┬───┬───┬───┬───┬───┬───┬───┐
  │   │   │   │   │   │   │   │   │
  └───┴───┴───┴───┴───┴───┴───┴───┘
                            │   │   └── PWM1CLKSEL
                            │   └────── PWM1CLKSEL
                            └────────── PWM1CLKSEL
                        ──────────────── Reserved
                    ──────────────────── PWM2CLKSEL
                ──────────────────────── PWM2CLKSEL
            ──────────────────────────── PWM2CLKSEL
        ──────────────────────────────── Reserved
```

Bit 7: Reserved

Bit 6-4: PWMOUT2 clock selection.

   The clock defined frequency is same as PWMOUT1 clock selection.

Bit 3: Reserved

Bit 2-0: PWMOUT1 clock Selection.

        <2:0> = 000: 46.87K Hz

        <2:0> = 001: 23.43K Hz (Default)

        <2:0> = 010: 11.72K Hz

        <2:0> = 011:   5.85K Hz

        <2:0> = 100:   2.93K Hz

**VBAT Monitor Control Register -- Index 5Dh (*Bank 0*)**

Register Location:        5Dh

Power on Default Value       00h

Attribute:        Read/Write

Size:        8 bits
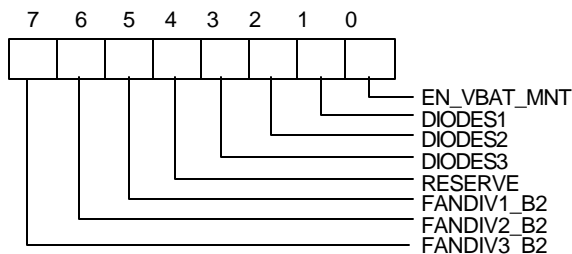


Bit 7: Fan3 divisor Bit 2.

Bit 6: Fan2 divisor Bit 2.

Bit 5: Fan1 divisor Bit 2.

Bit 4: Reserved.

Bit 3: Temperature sensor 3 select into thermal diode such as Pentium II CPU supported. Set to 1, select bipolar sensor. Set to 0, select thermistor sensor.

Bit 2: Sensor 2 type selection. Set to 1, select bipolar sensor. Set to 0, select thermistor sensor.

Bit 1: Sensor 1 type selection. Set to 1, select bipolar sensor. Set to 0, select thermistor sensor.

Bit 0: Set to 1, enable battery voltage monitor. Set to 0, disable battery voltage monitor. If enable this bit, the monitor value is value after one monitor cycle. Note that the monitor cycle time is at least 300ms for W83627HF hardware monitor.

**Fan divisor table :**

| Bit 2 | Bit 1 | Bit 0 | Fan Divisor | Bit 2 | Bit 1 | Bit 0 | Fan Divisor |
|-------|-------|-------|-------------|-------|-------|-------|-------------|
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 16 |
| 0 | 0 | 1 | 2 | 1 | 0 | 1 | 32 |
| 0 | 1 | 0 | 4 | 1 | 1 | 0 | 64 |
| 0 | 1 | 1 | 8 | 1 | 1 | 1 | 128 |

**Reserved Register -- 5Eh (*Bank 0*)**

**Reserved Register -- Index 5Fh (*Bank 0*)**

**Temperature Sensor 2 Temperature (High Byte) Register - Index 50h (*Bank 1*)**

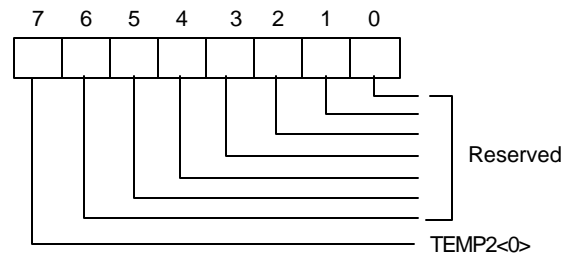Register Location:          50h

Attribute:                       Read Only
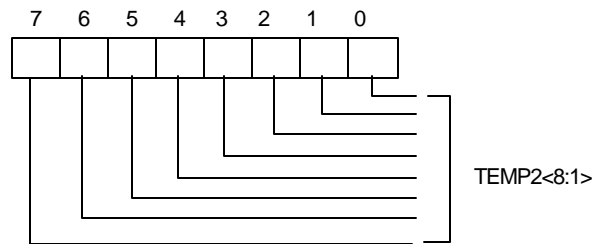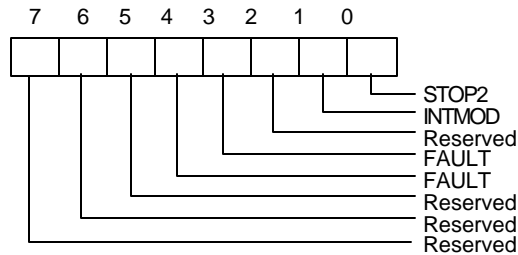
Size:                             8 bits



Bit 7: Temperature <8:1> of sensor 2, which is high byte.

**Temperature Sensor 2 Temperature (Low Byte) Register - Index 51h (*Bank 1*)**

Register Location:          51h

Attribute:                       Read Only

Size:                             8 bits



Bit 7: Temperature <0> of sensor2, which is low byte.

Bit 6-0: Reserved.

**Temperature Sensor 2 Configuration Register - Index 52h (*Bank 1*)**

Register Location:                52h

Power on Default Value            00h

Size:                             8 bits



Bit 7-5: Read  - Reserved. This bit should be set to 0.

Bit 4-3: Read/Write  - Number of faults to detect before setting OVT# output to avoid false tripping    due to noise.
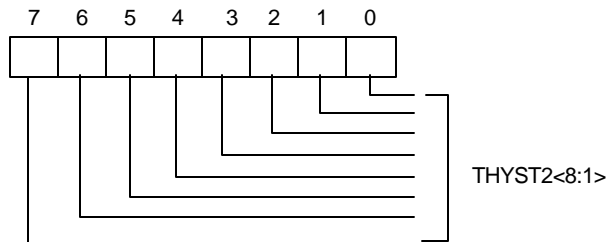
Bit 2: Read  - Reserved. This bit should be set to 0.

Bit 1: Read/Write  - OVT# Interrupt mode select. This bit default is set to 0, which is compared mode. When set to 1, interrupt mode will be selected.

Bit 0: Read/Write  - When set to 1 the sensor will stop monitor.


**Temperature Sensor 2 Hysteresis (High Byte) Register - Index 53h (*Bank 1*)**

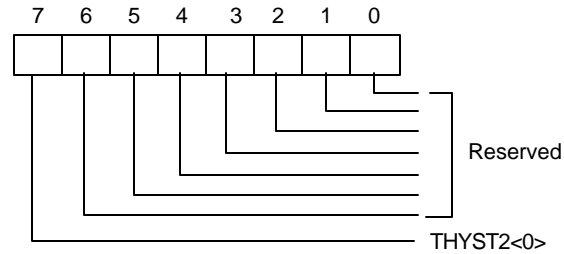Register Location:                53h

Power on Default Value            4Bh

Attribute:                        Read/Write

Size:                             8 bits



Bit 7-0: Temperature hysteresis bit 8-1, which is High Byte. The temperature default 75 degree C.

**Temperature Sensor 2 Hysteresis (Low Byte) Register - Index 54h (*Bank 1*)**

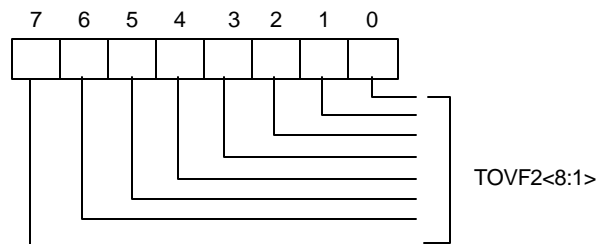| | |
|---|---|
| Register Location: | 54h |
| Power on Default Value | 00h |
| Attribute: | Read/Write |
| Size: | 8 bits |



Bit 7: Hysteresis temperature bit 0, which is low Byte.

Bit 6-0: Reserved.


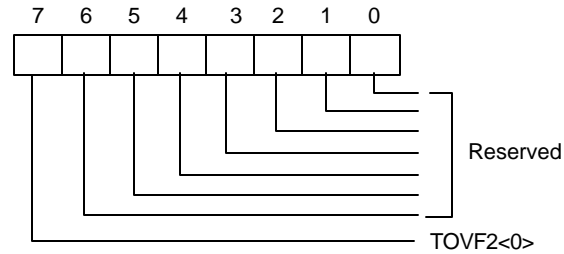**Temperature Sensor 2 Over-temperature (High Byte) Register - Index 55h (*Bank 1*)**

| | |
|---|---|
| Register Location: | 55h |
| Power on Default Value | 50h |
| Attribute: | Read/Write |
| Size: | 8 bits |



Bit 7-0: Over-temperature bit 8-1, which is High Byte. The temperature default 80 degree C.

**Temperature Sensor 2 Over-temperature (Low Byte) Register - Index 56h (*Bank 1*)**

Register Location:          56h

Power on Default Value      00h

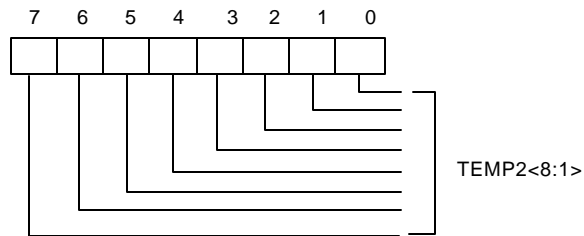Attribute:                  Read/Write

Size:                       8 bits



Bit 7: Over-temperature bit 0, which is low Byte.

Bit 6-0: Reserved.

**Temperature Sensor 3 Temperature (High Byte) Register - Index 50h (*Bank 2*)**
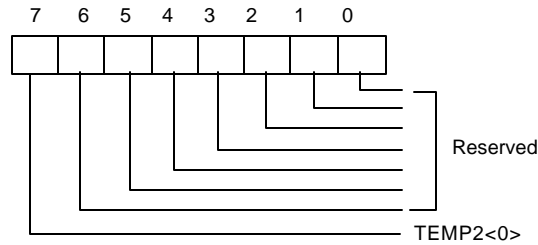
Register Location:      50h

Attribute:              Read Only

Size:                   8 bits



Bit 7-0: Temperature <8:1> of sensor 2, which is high byte.

**Temperature Sensor 3 Temperature (Low Byte) Register - Index 51h (*Bank 2*)**

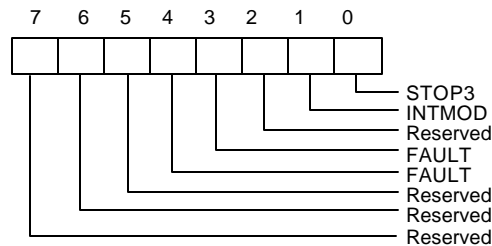Register Location:        51h

Attribute:                Read Only

Size:                     8 bits



Bit 7: Temperature <0> of sensor2, which is low byte.

Bit 6-0: Reserved.

**Temperature Sensor 3 Configuration Register - Index 52h (*Bank 2*)**

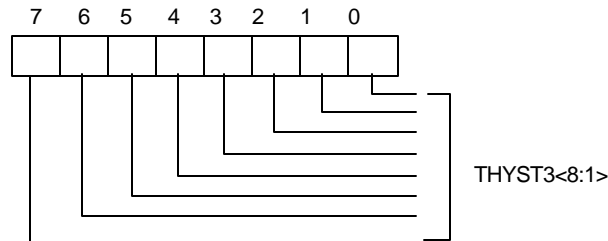Register Location:            52h

Power on Default Value        00h

Attribute:                    Read/Write

Size:                         8 bits



Bit 7-5: Read  - Reserved. This bit should be set to 0.

Bit 4-3: Read/Write  - Number of faults to detect before setting OVT# output to avoid false tripping    due to noise.

Bit 2: Read  - Reserved. This bit should be set to 0.

Bit 1: Read/Write  - OVT# Interrupt Mode select. This bit default is set to 0, which is Compared Mode. When   set to 1, Interrupt Mode will be selected.

Bit 0: Read/Write  - When set to 1 the sensor will stop monitor.

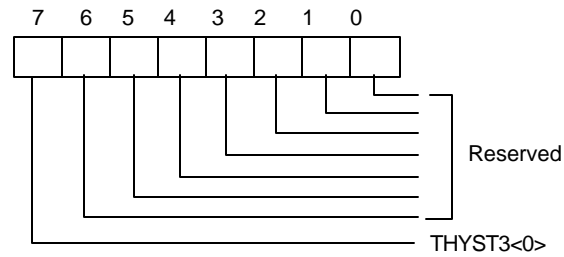**Temperature Sensor 3 Hysteresis (High Byte) Register - Index 53h (*Bank 2*)**

Register Location:          53h

Power on Default Value      4Bh

Attribute:                  Read/Write

Size:                       8 bits

```
      7   6   5   4   3   2   1   0
    ┌───┬───┬───┬───┬───┬───┬───┬───┐
    │   │   │   │   │   │   │   │   │
    └───┴───┴───┴───┴───┴───┴───┴───┘
                                        THYST3<8:1>
```

Bit 7-0: Temperature hysteresis bit 8-1, which is High Byte. The temperature default 75 degree C.


**Temperature Sensor 3 Hysteresis (Low Byte) Register - Index 54h (*Bank 2*)**

Register Location:          54h

Power on Default Value      00h

Attribute:                  Read/Write

Size:                       8 bits

```
      7   6   5   4   3   2   1   0
    ┌───┬───┬───┬───┬───┬───┬───┬───┐
    │   │   │   │   │   │   │   │   │
    └───┴───┴───┴───┴───┴───┴───┴───┘
                                        Reserved

                                        THYST3<0>
```
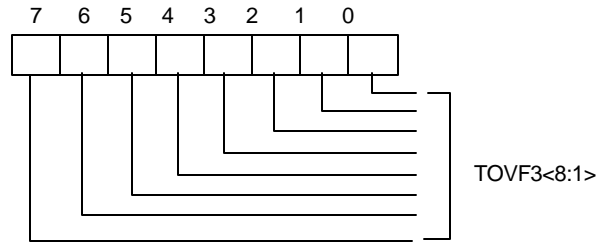
Bit 7: Hysteresis temperature bit 0, which is low Byte.

Bit 6-0: Reserved.

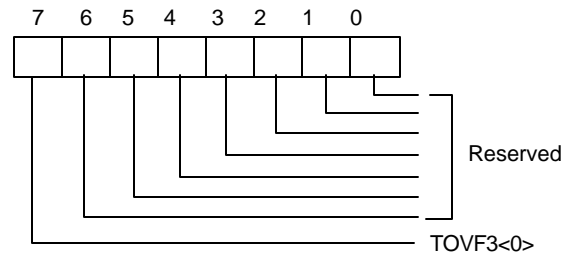**Temperature Sensor 3 Over-temperature (High Byte) Register - Index 55h (*Bank 2*)**

| | |
|---|---|
| Register Location: | 55h |
| Power on Default Value | 50h |
| Attribute: | Read/Write |
| Size: | 8 bits |

```
  7   6   5   4   3   2   1   0
┌───┬───┬───┬───┬───┬───┬───┬───┐
│   │   │   │   │   │   │   │   │
└───┴───┴───┴───┴───┴───┴───┴───┘

                          TOVF3<8:1>
```

Bit 7-0: Over-temperature bit 8-1, which is High Byte. The temperature default 80 degree C.

**Temperature Sensor 3 Over-temperature (Low Byte) Register - Index 56h(*Bank 2*)**

| | |
|---|---|
| Register Location: | 56h |
| Power on Default Value | 00h |
| Attribute: | Read/Write |
| Size: | 8 bits |

```
  7   6   5   4   3   2   1   0
┌───┬───┬───┬───┬───┬───┬───┬───┐
│   │   │   │   │   │   │   │   │
└───┴───┴───┴───┴───┴───┴───┴───┘

                          Reserved

                     TOVF3<0>
```
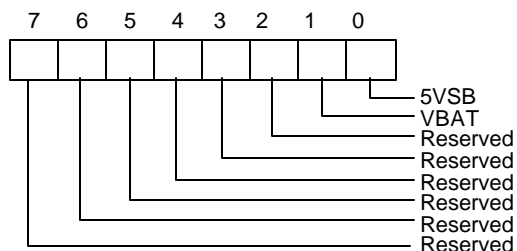
Bit 7: Over-temperature bit 0, which is low Byte.

Bit 6-0: Reserved.

**Interrupt Status Register 3 -- Index 50h (BANK4)**

Register Location:                50h

Power on Default Value            00h

Attribute:                        Read Only
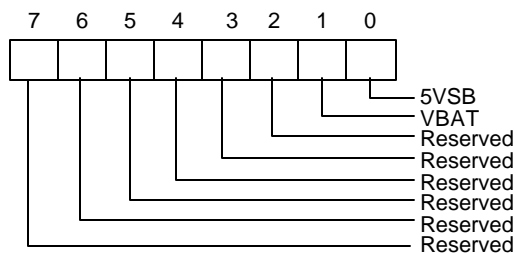
Size:                             8 bits



Bit 7-2: Reserved.

Bit 1: A one indicates a High or Low limit of VBAT has been exceeded.

Bit 0: A one indicates a High or Low limit of 5VSB has been exceeded.


**SMI# Mask Register 3 --  Index 51h (BANK 4)**

Register Location:                51h

Power on Default Value            00h

Attribute:                        Read/Write

Size:                             8 bits
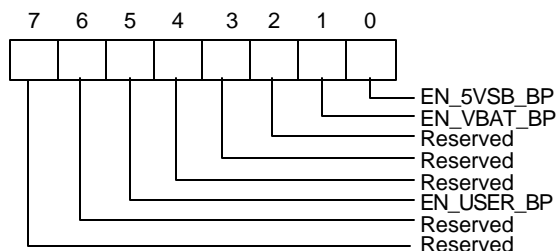


Bit 7-2: Reserved.

Bit 1: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

Bit 0: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.


**Reserved Register -- Index 52h (*Bank 4*)**

**BEEP Control Register 3-- Index 53h (*Bank 4*)**

Register Location:          53h

Power on Default Value      00h

Attribute:                  Read/Write

Size:                       8 bits

```
  7   6   5   4   3   2   1   0
┌───┬───┬───┬───┬───┬───┬───┬───┐
│   │   │   │   │   │   │   │   │
└───┴───┴───┴───┴───┴───┴───┴───┘
                          │   └── EN_5VSB_BP
                          └────── EN_VBAT_BP
                      ──────────── Reserved
                  ────────────────── Reserved
              ────────────────────── Reserved
          ────────────────────────── EN_USER_BP
      ────────────────────────────── Reserved
  ────────────────────────────────── Reserved
```

Bit 7-6: Reserved.

Bit 5: User define BEEP output function. Write 1, the BEEP is always active. Write 0, this function is inactive. (Default 0)
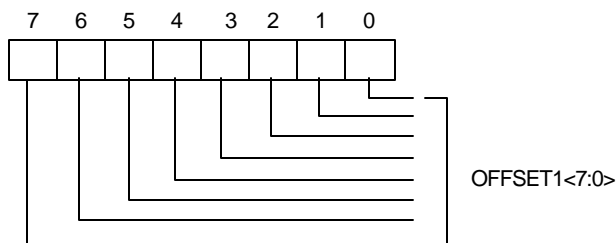
Bit 4-2: Reserved.

Bit 1: Enable BEEP output from VBAT. Write 1, enable BEEP output, which is default value.

Bit 0: Enable BEEP Output from 5VSB. Write 1, enable BEEP output, which is default value.

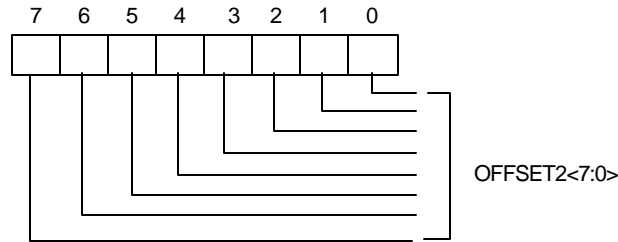**Temperature Sensor 1 Offset Register -- Index 54h (*Bank 4*)**

Register Location:          54h

Power on Default Value      00h

Attribute:                  Read/Write

Size:                       8 bits

```
  7   6   5   4   3   2   1   0
┌───┬───┬───┬───┬───┬───┬───┬───┐
│   │   │   │   │   │   │   │   │
└───┴───┴───┴───┴───┴───┴───┴───┘
                                    OFFSET1<7:0>
```

Bit 7-0: Temperature 1 base temperature. The temperature is added by both monitor value and offset value.

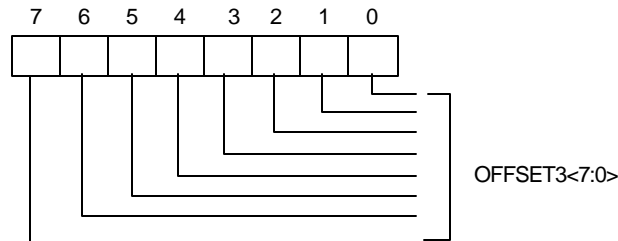**Temperature Sensor 2 Offset Register -- Index 55h (*Bank 4*)**

Register Location:          55h

Power on Default Value      00h

Attribute:                  Read/Write

Size:                       8 bits



OFFSET2<7:0>

Bit 7-0: Temperature 2 base temperature. The temperature is added by both monitor value and offset value.

**Temperature Sensor 3 Offset Register -- Index 56h (*Bank 4*)**

Register Location:          56h

Power on Default Value      00h

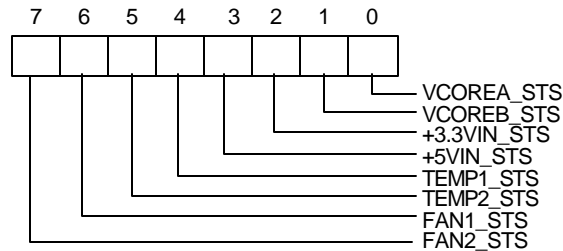Attribute:                  Read/Write

Size:                       8 bits



OFFSET3<7:0>

Bit 7-0: Temperature 3 base temperature. The temperature is added by both monitor value and offset value.

**Reserved Register -- Index 57h--58h**

**Real Time Hardware Status Register I -- Index 59h (*Bank 4*)**

Register Location:             59h

Power on Default Value         00h

Attribute:                     Read Only

Size:                          8 bits

```
    7   6   5   4   3   2   1   0
  ┌───┬───┬───┬───┬───┬───┬───┬───┐
  │   │   │   │   │   │   │   │   │
  └───┴───┴───┴───┴───┴───┴───┴───┘
                            └─────── VCOREA_STS
                        └─────────── VCOREB_STS
                    └─────────────── +3.3VIN_STS
                └─────────────────── +5VIN_STS
            └─────────────────────── TEMP1_STS
        └─────────────────────────── TEMP2_STS
    └─────────────────────────────── FAN1_STS
  └─────────────────────────────────FAN2_STS
```

Bit 7: FAN 2 Status. Set 1, the fan speed counter is over the limit value. Set 0, the fan speed counter is in the limit range.

Bit 6: FAN 1 Status. Set 1, the fan speed counter is over the limit value. Set 0, the fan speed counter is in the limit range.

Bit 5: Temperature sensor 2 Status. Set 1, the voltage of temperature sensor is over the limit value. Set 0, the voltage of temperature sensor is in the limit range.

Bit 4: Temperature sensor 1 Status. Set 1, the voltage of temperature sensor is over the limit value. Set 0, the voltage of temperature sensor is in the limit range.

Bit 3: +5V Voltage Status. Set 1, the voltage of +5V is over the limit value. Set 0, the voltage of +5V is in the limit range.
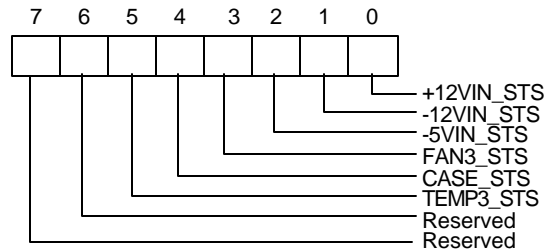
Bit 2: +3.3V Voltage Status. Set 1, the  voltage of +3.3V is over the limit value. Set 0, the voltage of +3.3V is in the limit range.

Bit 1: VCOREB Voltage Status. Set 1, the voltage of VCOREB is over the limit value. Set 0, the voltage of VCOREB is in the limit range.

Bit 0: VCOREA Voltage Status. Set 1, the voltage of VCORE A is over the limit value. Set 0, the voltage of VCORE A is in the limit range.

**Real Time Hardware Status Register II -- Index 5Ah (*Bank 4*)**

Register Location:              5Ah

Power on Default Value          00h

Attribute:                      Read Only

Size:                           8 bits



Bit 7-6: Reserved

Bit 5: Temperature sensor 3 Status. Set 1, the voltage of temperature sensor is over the limit value. Set 0, the voltage of temperature sensor is in the limit range.

Bit 4: Case Open Status. Set 1, the case open sensor is sensed the high value. Set 0

Bit 3: FAN3 Voltage Status. Set 1, the fan speed counter is over the limit value. Set 0, the fan speed counter is during the limit range.
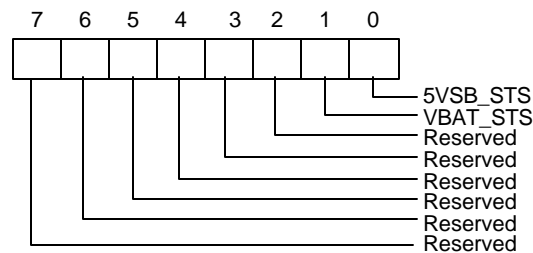
Bit 2: -5V Voltage Status. Set 1, the voltage of -5V is over the limit value. Set 0, the voltage of -5V is during the limit range.

Bit 1: -12V Voltage Status. Set 1, the voltage of -12V is over the limit value. Set 0, the voltage of - 12V is during the limit range.

Bit 0: +12V Voltage Status. Set 1, the voltage of +12V is over the limit value. Set 0, the voltage of +12V is in the limit range.

**Real Time Hardware Status Register III -- Index 5Bh (*Bank 4*)**

Register Location:              5Bh

Power on Default Value          00h

Attribute:                      Read Only

Size:                           8 bits
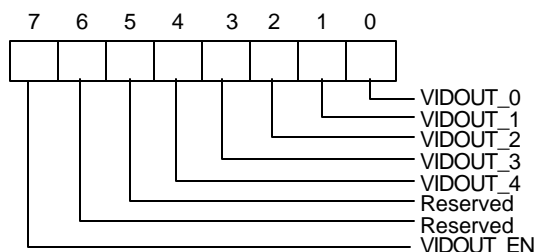


Bit 7-2: Reserved.

Bit 1: VBAT Voltage Status. Set 1, the voltage of VBAT is over the limit value. Set 0, the voltage of VBAT is during the limit range.

Bit 0: 5VSB Voltage Status. Set 1, the voltage of 5VSB is over the limit value. Set 0, the voltage of 5VSB is in the limit range.

**Reserved Register -- Index 5Ch (*Bank 4*)**

**VID Output Register -- Index 5Dh (*Bank 4*)**

Register Location:          5Dh

Power on Default Value  <7:0> = 0000,0000h

Attribute:                  Read/Write

Size:                       8 bits

```
 7   6   5   4   3   2   1   0
┌───┬───┬───┬───┬───┬───┬───┬───┐
│   │   │   │   │   │   │   │   │
└───┴───┴───┴───┴───┴───┴───┴───┘
                        └── VIDOUT_0
                      └──── VIDOUT_1
                  └──────── VIDOUT_2
              └──────────── VIDOUT_3
          └──────────────── VIDOUT_4
      └────────────────────  Reserved
  └────────────────────────  Reserved
  └──────────────────────── VIDOUT_EN
```

Bit 7: VID Output Enable. Set 1, enable VID pins to output. Set 0, disable VID pins to output. Default is 0.

Bit 6-5: Reserved.

Bit 4-0: Set 1, VID pins drive a 1 . Set 0, VID pins drive a 0. Default is 0.

**Value RAM 2¾ Index 50h - 5Ah (auto-increment)  *(BANK 5)***

| Address A6-A0 Auto-Increment | Description |
|---|---|
| 50h | 5VSB reading |
| 51h | VBAT reading |
| 52h | Reserved |
| 53h | Reserved |
| 54h | 5VSB High Limit |
| 55h | 5VSB Low Limit. |
| 56h | VBAT High Limit |
| 57h | VBAT Low Limit |

**Winbond Test Register -- Index 50h (*Bank 6*)**

## 3. SERIAL IRQ

W83627HF supports a serial IRQ scheme. This allow a signal line to be used to report the legacy ISA interrupt rerquests. Because more than one device may need to share the signal serial IRQ signal line, an open drain signal scheme is used. The clock source is the PCI clock. The serial interrupt is transfered on the IRQSER signal, one cycle consisting of three frames types: a start frame, several IRQ/Data frame, and one Stop frame.

### 3.1 Start Frame

There are two modes of operation for the IRQSER Start frame: Quiet mode and Continuous mode.

In the Quiet mode, the peripheral drives the SERIRQ signal active low for one clock, and then tri-states it. This brings all the states machines of the peripherals from idle to active states. The host controller will then take over driving IRQSER signal low in the next clock and will continue driving the IRQSER low for programmable 3 to 7 clock periods. This makes the total number of clocks low for 4 to 8 clock periods. After these clocks, the host controller will drive the IRQSER high for one clock and then tri-states it.

In the Continuous mode, only the host controller initiates the START frame to update IRQ/Data line information. The host controller drives the IRQSER signal low for 4 to 8 clock periods. Upon a reset, the IRQSER signal is defaulted to the Continuous mode for the host controller to initiate the first Start frame.

### 3.2 IRQ/Data Frame

Once the start frame has been initiated, all the peripherals must start counting frames based on the rsing edge of the start pulse. Each IRQ/Data Frame is three clocks: Sample phase, Recovery phase, and Turn-around phase.

During the Sample phase, the peripheral drives SERIRQ low if the corresponding IRQ is active. If the corresponding IRQ is inactive, then IRQSER must be left tri-stated. During the Recovery phase, the peripheral device drives the IRQSER high. During the Turn-around phase, the peripheral device left the IRQSER tri-stated.

The IRQ/Data Frame has a number of specific order, as shown in Table 3-1.

Table 3-1 IRQSER Sampling periods

| IRQ/Data Frame | Signal Sampled | # of clocks past Start |
|:---:|:---:|:---:|
| 1 | IRQ0 | 2 |
| 2 | IRQ1 | 5 |
| 3 | $\overline{SMI}$ | 8 |
| 4 | IRQ3 | 11 |
| 5 | IRQ4 | 14 |
| 6 | IRQ5 | 17 |
| 7 | IRQ6 | 20 |
| 8 | IRQ7 | 23 |
| 9 | IRQ8 | 26 |
| 10 | IRQ9 | 29 |
| 11 | IRQ10 | 32 |
| 12 | IRQ11 | 35 |
| 13 | IRQ12 | 38 |
| 14 | IRQ13 | 41 |
| 15 | IRQ14 | 44 |
| 16 | IRQ15 | 47 |
| 17 | $\overline{IOCHCK}$ | 50 |
| 18 | $\overline{INTA}$ | 53 |
| 19 | $\overline{INTB}$ | 56 |
| 20 | $\overline{INTC}$ | 59 |
| 21 | $\overline{INTD}$ | 62 |
| 32:22 | Unassigned | 95 |

## 3.3 Stop Frame

After all IRQ/Data Frames have completed, the host controller will terminate IRQSER by a Stop frame. Only the host controller can initiate the Stop frame by driving IRQSER low for 2 or 3 clocks. If the Stop Frame is low for 2 clocks, the next IRQSER cycle's Sample mode is the Quiet mode. If the Stop Frame is low for 3 clocks, the next IRQSER cycle's Sample mode is the Continuous mode.

# 4. CONFIGURATION REGISTER

## 4.1 Chip (Global) Control Register

**CR02 (Default 0x00)**

Bit 7 - 1 : Reserved.

Bit 0 : SWRST --> Soft Reset.

**CR07**

Bit 7 - 0 : LDNB7 - LDNB0 --> Logical Device Number Bit 7 - 0

**CR20**

Bit 7 - 0 : DEVIDB7 - DEBIDB0 --> Device ID Bit 7 - Bit 0 = 0x52 (read only).

**CR21**

Bit 7 - 0 : DEVREVB7 - DEBREVB0 --> Device Rev Bit 7 - Bit 0 = 0x17 (read only, G version).

Bit 7 - 0 : DEVREVB7 - DEBREVB0 --> Device Rev Bit 7 - Bit 0 = 0x3A (read only, J version).

**CR22 (Default 0xff)**

Bit 7 : Reserved.

Bit 6 : HMPWD

    = 0 Power down

    = 1 No Power down

Bit 5 : URBPWD

    = 0 Power down

    = 1 No Power down

Bit 4 : URAPWD

    = 0 Power down

    = 1 No Power down

Bit 3 : PRTPWD

    = 0 Power down

    = 1 No Power down

Bit 2, 1 : Reserved.

Bit 0 : FDCPWD

    = 0 Power down

    = 1 No Power down

**CR23 (Default 0x00)**

Bit 7 - 1 : Reserved.

Bit 0 : IPD (Immediate Power Down). When set to 1, it will put the whole chip into power down mode immediately.

**CR24 (Default 0b1s000s0s)**

Bit 7 : EN16SA

= 0 12 bit Address Qualification

= 1 16 bit Address Qualification

Bit 6 :CLKSEL

= 0 The clock input on Pin 1 should be 24 Mhz.

= 1 The clock input on Pin 1 should be 48 Mhz.

The corresponding power-on setting pin is SOUTB (pin 83).

Bit 5 - 3 : Reserved

Bit 2 : ENKBC

= 0 KBC is disabled after hardware reset.

= 1 KBC is enabled after hardware reset.

This bit is read only, and set/reset by power-on setting pin. The corresponding power-on setting pin is SOUTA (pin 54).

Bit 1 : Reserved

Bit 0 : PNPCVS

= 0 The Compatible PnP address select registers have default values.

= 1 The Compatible PnP address select registers have no default value.

When trying to make a change to this bit, new value of PNPCVS must be complementary to the old one to make an effective change. For example, the user must set PNPCVS to 0 first and then reset it to 1 to reset these PnP registers if the present value of PNPCVS is 1. The corresponding power-on setting pin is NDTRA (pin 52).

**CR25 (Default 0x00)**

Bit 7 - 6 : Reserved

Bit 5 : URBTRI

Bit 4 : URATRI

Bit 3 : PRTTRI

Bit 2 - 1 : Reserved

Bit 0 : FDCTRI.

**CR26 (Default 0b0s000000)**

Bit 7 : SEL4FDD

= 0 Select two FDD mode.

= 1 Select four FDD mode.

Bit 6 : HEFRAS

These two bits define how to enable Configuration mode. The corresponding power-on setting pin is NRTSA (pin 51).

HEFRAS Address and Value

= 0 Write 87h to the location 2E twice.

= 1 Write 87h to the location 4Etwice.

Bit 5 : LOCKREG

= 0 Enable R/W Configuration Registers

= 1 Disable R/W Configuration Registers.

Bit 4 :Reserve

Bit 3 : DSFDLGRQ

= 0 Enable FDC legacy mode on IRQ and DRQ selection, then DO register bit 3 is effective on selecting IRQ

= 1 Disable FDC legacy mode on IRQ and DRQ selection, then DO register bit 3 is not effective on selecting IRQ

Bit 2 : DSPRLGRQ

= 0 Enable PRT legacy mode on IRQ and DRQ selection, then DCR bit 4 is effective on selecting IRQ

= 1 Disable PRT legacy mode on IRQ and DRQ selection, then DCR bit 4 is not effective on selecting IRQ

Bit 1 : DSUALGRQ

= 0 Enable UART A legacy mode IRQ selecting, then MCR bit 3 is effective on selectingIRQ

= 1 Disable UART A legacy mode IRQ selecting, then MCR bit 3 is not effective on selecting IRQ

Bit 0 : DSUBLGRQ

= 0 Enable UART B legacy mode IRQ selecting, then MCR bit 3 is effective on selecting IRQ

= 1 Disable UART B legacy mode IRQ selecting, then MCR bit 3 is not effective on selecting IRQ

**CR28 (Default 0x00)**

Bit 7 - 3 : Reserved.

Bit 2 - 0 : PRTMODS2 - PRTMODS0

= 0xx  Parallel Port Mode

= 100  Reserved

= 101  External FDC Mode

= 110  Reserved

= 111  External two FDC Mode

**CR29 (GPIO3 multiplexed pin selection register.  VBAT powered.  Default 0x00)**

Bit 7        : PIN64S

= 0    SUSLED (SUSLED control bits are in CRF3 of Logical Device 9)

= 1    GP35

Bit 6        : PIN69S

= 00   CIRRX#

= 01   GP34

Bit 5        : PIN70S

= 0    RSMRST#

= 1    GP33

Bit 4        : PIN71S

= 0    PWROK

= 1    GP32

Bit 3        : PIN72S

= 0    PWRCTL#

= 1    GP31

Bit 2        : PIN 73S

= 0    SLP_SX#

= 1    GP30

Bit 1        : Reserved

Bit 0        : Reserved

**CR2A (GPIO multiplexed pin selection register 1.  VCC powered.  Default 0X7C)**

Bit 7 : Port Select (select Game Port or General Purpose I/O Port 1)

= 0   Game Port

= 1   General Purpose I/O Port 1 (pin121~128 select function GP10~GP17 or KBC Port 1)

Bit 6 : PIN128S

= 0   8042 P12

= 1   GP10

Bit 5 : PIN127S

= 0   8042 P13

= 1   GP11

Bit 4 : PIN126S

= 0   8042 P14

= 1   GP12

Bit 3 : PIN125S

= 0   8042 P15

= 1   GP13

Bit 2 : PIN124S

= 0   8042 P16

= 1   GP14

Bit 1 : PIN120S

= 0   MSO (MIDI  Serial Output)

= 1   IRQIN0 (select IRQ resource through CRF4 Bit 7-4 of Logical Device 8)

Bit 1 : PIN119S

= 0   MS1 (MIDI  Serial Input)

= 1   GP20

**CR2B(GPIO multiplexed pin selection register 2.  VCC powered.  Default 0XC0)**

Bit 7 :PIN92S

= 0   SCL

= 1   GP21

Bit 6 :PIN91S

= 0   SDA

= 1   GP22

Bit 5 : PIN90S

= 0   PLED (PLED0 control bits are in CRF5 of Logical Device 8)

= 1   GP23

Bit 4     : PIN89S

          = 0 WDTO (Watch Dog Timer is controlled by CRF5, CRF6, CRF7 of Logical Device 8)

          = 1 GP24

Bit 3     : PIN88S

          = 0 IRRX

          = 1 GP25

Bit 2     : PIN87S

          = 0 IRTX

          = 1 GP26

Bit 1-0   : PIN 2S

          = 00 DRVDEN1

          = 01 IRQIN1 (select IRQ resource through CRF4 Bit 7-4 of Logical Device8) SMI# (For D version only)

          = 10 Reserved

          = 11 GP27

**CR2C (Default 0x00)**

   Reserved

**CR2E (Default 0x00)**

   Test Modes: Reserved for Winbond.

**CR2F (Default 0x00)**

   Test Modes: Reserved for Winbond.

## 4.2 Logical Device 0 (FDC)

**CR30 (Default 0x01 if PNPCVS = 0 during POR, default 0x00 otherwise)**

   Bit 7 - 1  : Reserved.

   Bit 0     = 1 Activates the logical device.

             = 0 Logical device is inactive.

**CR60, CR 61 (Default 0x03, 0xf0 if PNPCVS = 0 during POR, default 0x00, 0x00 otherwise)**

   These two registers select FDC I/O base address [0x100:0xFF8] on 8 bytes boundary.

**CR70 (Default 0x06 if PNPCVS = 0 during POR, default 0x00 otherwise)**

    Bit 7 - 4  : Reserved.

    Bit 3 - 0  : These bits select IRQ resource for FDC.


**CR74 (Default 0x02 if PNPCVS = 0 during POR, default 0x04 otherwise)**

    Bit 7 - 3  : Reserved.

    Bit 2 - 0  : These bits select DRQ resource for FDC.

            = 0x00 DMA0

            = 0x01 DMA1

            = 0x02 DMA2

            = 0x03 DMA3

            = 0x04 - 0x07 No DMA active


**CRF0 (Default 0x0E)**

**FDD Mode Register**

    Bit 7     : FIPURDWN

This bit controls the internal pull-up resistors of the FDC input pins RDATA, INDEX, TRAK0, DSKCHG, and WP.

            = 0    The internal pull-up resistors of FDC are turned on.(Default)

            = 1    The internal pull-up resistors of FDC are turned off.

    Bit 6     : INTVERTZ

This bit determines the polarity of all FDD interface signals.

            = 0    FDD interface signals are active low.

            = 1    FDD interface signals are active high.

    Bit 5     : DRV2EN (PS2 mode only)

When this bit is a logic 0, indicates a second drive is installed and is reflected in status register A.

    Bit 4     : Swap Drive 0, 1 Mode

            = 0    No Swap (Default)

            = 1    Drive and Motor sel 0 and 1 are swapped.

    Bit 3 - 2 :Interface Mode

            = 11   AT Mode (Default)

            = 10   (Reserved)

            = 01   PS/2

            = 00   Model 30

    Bit 1     : FDC DMA Mode

            = 0   Burst Mode is enabled

            = 1   Non-Burst Mode (Default)

    Bit 0     : Floppy Mode

            = 0   Normal Floppy Mode (Default)

            = 1   Enhanced 3-mode FDD

**CRF1 (Default 0x00)**

Bit 7 - 6 : Boot Floppy

= 00   FDD A

= 01   FDD B

= 10   FDD C

= 11   FDD D

Bit 5, 4   : Media ID1, Media ID0. These bits will be reflected on FDC's Tape Drive Register bit 7, 6.

Bit 3 - 2   : Density Select

= 00   Normal (Default)

= 01   Normal

= 10   1 (Forced to logic 1)

= 11   0 (Forced to logic 0)

Bit 1      : DISFDDWR

= 0 Enable FDD write.

= 1 Disable FDD write(forces pins WE, WD stay high).

Bit 0      : SWWP

= 0 Normal, use WP to determine whether the FDD is write protected or not.

= 1 FDD is always write-protected.

**CRF2 (Default 0xFF)**

Bit 7 - 6   : FDD D Drive Type

Bit 5 - 4   : FDD C Drive Type

Bit 3 - 2   : FDD B Drive Type

Bit 1 - 0   : FDD A Drive Type

**CRF4 (Default 0x00)**

**FDD0 Selection:**

Bit 7      : Reserved.

Bit 6      : Precomp. Disable.

= 1    Disable FDC Precompensation.

= 0    Enable FDC Precompensation.

Bit 5      : Reserved.

Bit 4 - 3   : DRTS1, DRTS0: Data Rate Table select (Refer to TABLE A).

= 00 Select Regular drives and 2.88 format

= 01 3-mode drive

= 10 2 Meg Tape

= 11 Reserved

Bit 2      : Reserved.

Bit 1:0    : DTYPE0, DTYPE1: Drive Type select (Refer to TABLE B).

**CRF5 (Default 0x00)**

FDD1 Selection: Same as FDD0 of CRF4.

**TABLE A**

| Drive Rate Table Select | | Data Rate | | Selected Data Rate | | SELDEN |
|---|---|---|---|---|---|---|
| DRTS1 | DRTS0 | DRATE1 | DRATE0 | MFM | FM | |
| 0 | 0 | 1 | 1 | 1Meg | --- | 1 |
| | | 0 | 0 | 500K | 250K | 1 |
| | | 0 | 1 | 300K | 150K | 0 |
| | | 1 | 0 | 250K | 125K | 0 |
| 0 | 1 | 1 | 1 | 1Meg | --- | 1 |
| | | 0 | 0 | 500K | 250K | 1 |
| | | 0 | 1 | 500K | 250K | 0 |
| | | 1 | 0 | 250K | 125K | 0 |
| 1 | 0 | 1 | 1 | 1Meg | --- | 1 |
| | | 0 | 0 | 500K | 250K | 1 |
| | | 0 | 1 | 2Meg | --- | 0 |
| | | 1 | 0 | 250K | 125K | 0 |

**TABLE B**

| DTYPE0 | DTYPE1 | DRVDEN0(pin 2) | DRVDEN1(pin 3) | DRIVE TYPE |
|---|---|---|---|---|
| 0 | 0 | SELDEN | DRATE0 | 4/2/1 MB 3.5"" <br> 2/1 MB 5.25" <br> 2/1.6/1 MB 3.5" (3-MODE) |
| 0 | 1 | DRATE1 | DRATE0 | |
| 1 | 0 | $\overline{\text{SELDEN}}$ | DRATE0 | |
| 1 | 1 | DRATE0 | DRATE1 | |

## 4.3 Logical Device 1 (Parallel Port)

**CR30 (Default 0x01 if PNPCVS = 0 during POR, default 0x00 otherwise)**

    Bit 7 - 1  : Reserved.

    Bit 0      = 1 Activates the logical device.

              = 0 Logical device is inactive.

**CR60, CR 61 (Default 0x03, 0x78 if PNPCVS = 0 during POR, default 0x00, 0x00 otherwise )**

    These two registers select Parallel Port I/O base address.

    [0x100:0xFFC] on 4 byte boundary (EPP not supported) or

    [0x100:0xFF8] on 8 byte boundary(all modes supported, EPP is only available when the base address is on 8 byte boundary).

**CR70 (Default 0x07 if PNPCVS = 0 during POR, default 0x00 otherwise)**

    Bit 7 - 4  : Reserved.

    Bit [3:0]  : These bits select IRQ resource for Parallel Port.

**CR74 (Default 0x04)**

    Bit 7 - 3  : Reserved.

    Bit 2 - 0  : These bits select DRQ resource for Parallel Port.

                 0x00=DMA0

                 0x01=DMA1

                 0x02=DMA2

                 0x03=DMA3

                 0x04 - 0x07= No DMA active

**CRF0 (Default 0x3F)**

    Bit 7     : Reserved.

    Bit 6 - 3  : ECP FIFO Threshold.

    Bit 2 - 0  : Parallel Port Mode (CR28 PRTMODS2 = 0)

            = 100   Printer Mode (Default)

            = 000   Standard and Bi-direction (SPP) mode

            = 001   EPP - 1.9 and SPP mode

            = 101   EPP - 1.7 and SPP mode

            = 010   ECP mode

            = 011   ECP and EPP - 1.9 mode

            = 111   ECP and EPP - 1.7 mode.

## 4.4 Logical Device 2 (UART A)

**CR30 (Default 0x01 if PNPCVS = 0 during POR, default 0x00 otherwise)**
  Bit 7 - 1  : Reserved.
  Bit 0    = 1 Activates the logical device.
      = 0 Logical device is inactive.

**CR60, CR 61 (Default 0x03, 0xF8 if PNPCVS = 0 during POR, default 0x00, 0x00 otherwise)**
  These two registers select Serial Port 1 I/O base address [0x100:0xFF8] on 8 byte boundary.

**CR70 (Default 0x04 if PNPCVS = 0 during POR, default 0x00 otherwise)**
  Bit 7 - 4  : Reserved.
  Bit 3 - 0  : These bits select IRQ resource for Serial Port 1.

**CRF0 (Default 0x00)**
  Bit 7 - 2  : Reserved.
  Bit 1 - 0  : SUACLKB1, SUACLKB0
      = 00    UART A clock source is 1.8462 Mhz (24MHz/13)
      = 01    UART A clock source is 2 Mhz (24MHz/12)
      = 10    UART A clock source is 24 Mhz (24MHz/1)
      = 11    UART A clock source is 14.769 Mhz (24mhz/1.625)

## 4.5 Logical Device 3 (UART B)

**CR30 (Default 0x01 if PNPCVS = 0 during POR, default 0x00 otherwise)**
  Bit 7 - 1  : Reserved.
  Bit 0    = 1 Activates the logical device.
      = 0 Logical device is inactive.

**CR60, CR 61 (Default 0x02, 0xF8 if PNPCVS = 0 during POR, default 0x00, 0x00 otherwise)**
  These two registers select Serial Port 2 I/O base address [0x100:0xFF8] on 8 byte boundary.

**CR70 (Default 0x03 if PNPCVS = 0 during POR, default 0x00 otherwise)**
  Bit 7 - 4  : Reserved.
  Bit [3:0]  : These bits select IRQ resource for Serial Port 2.

**CRF0 (Default 0x00)**

Bit 7 - 4  : Reserved.

Bit 3      : RXW4C

= 0 No reception delay when IR is changed from TX mode to RX mode.

= 1 Reception delays 4 characters time (40 bit-time) when SIR is changed from TX mode to RX mode.

Bit 2      : TXW4C

= 0 No transmission delay when SIR is changed from RX mode to TX mode.

= 1 Transmission delays 4 characters time (40 bit-time) when SIR is changed from RX mode to TX mode.

Bit 1 - 0  : SUBCLKB1, SUBCLKB0

= 00    UART B clock source is 1.8462 Mhz (24MHz/13)

= 01    UART B clock source is 2 Mhz (24MHz/12)

= 10    UART B clock source is 24 Mhz (24MHz/1)

= 11    UART B clock source is 14.769 Mhz (24mhz/1.625)

**CRF1 (Default 0x00)**

Bit 7      : Reserved.

Bit 6      : IRLOCSEL.  IR I/O pins' location select.

= 0Through SINB/SOUTB.

= 1Through IRRX/IRTX.

Bit 5      : IRMODE2.  IR function mode selection bit 2.

Bit 4      : IRMODE1.  IR function mode selection bit 1.

Bit 3      : IRMODE0.  IR function mode selection bit 0.

| IR MODE | IR FUNCTION | IRTX | IRRX |
|---------|-------------|------|------|
| 00X | Disable | tri-state | high |
| 010* | IrDA | Active pulse 1.6 $\mu$S | Demodulation into SINB/IRRX |
| 011* | IrDA | Active pulse 3/16 bit time | Demodulation into SINB/IRRX |
| 100 | ASK-IR | Inverting IRTX/SOUTB pin | routed to SINB/IRRX |
| 101 | ASK-IR | Inverting IRTX/SOUTB & 500 KHZ clock | routed to SINB/IRRX |
| 110 | ASK-IR | Inverting IRTX/SOUTB | Demodulation into SINB/IRRX |
| 111* | ASK-IR | Inverting IRTX/SOUTB & 500 KHZ clock | Demodulation into SINB/IRRX |

Note: The notation is normal mode in the IR function.

Bit 2    : HDUPLX.  IR half/full duplex function select.

          = 0The IR function is Full Duplex.

          = 1The IR function is Half Duplex.

Bit 1    : TX2INV

          = 0the SOUTB pin of UART B function or IRTX pin of IR function in normal condition.

          = 1inverse the SOUTB pin of UART B function or IRTX pin of IR function.

Bit 0    : RX2INV.

          = 0the SINB pin of  UART B function or IRRX pin of IR function in normal condition.

          = 1inverse the SINB pin of  UART B function or IRRX pin of IR function

## 4.6 Logical Device 5 (KBC)

**CR30 (Default 0x01 if PNPCVS = 0 during POR, default 0x00 otherwise)**

    Bit 7 - 1  : Reserved.

    Bit 0    = 1 Activates the logical device.

              = 0 Logical device is inactive.

**CR60, CR 61 (Default 0x00, 0x60 if PNPCVS = 0 during POR, default 0x00 otherwise)**

    These two registers select the first KBC I/O base address [0x100:0xFFF] on 1 byte boundary.

**CR62, CR 63 (Default 0x00, 0x64 if PNPCVS = 0 during POR, default 0x00 otherwise)**

    These two registers select the second KBC I/O base address [0x100:0xFFF] on 1 byte boundary.

**CR70 (Default 0x01 if PNPCVS = 0 during POR, default 0x00 otherwise)**

    Bit 7 - 4  : Reserved.

    Bit [3:0]  : These bits select IRQ resource for KINT (keyboard).

**CR72 (Default 0x0C if PNPCVS = 0 during POR, default 0x00 otherwise)**

    Bit 7 - 4  : Reserved.

    Bit [3:0]  : These bits select IRQ resource for MINT (PS2 Mouse)

**CRF0 (Default 0x80)**

    Bit 7 - 6  : KBC clock rate selection

               = 00 Select 6MHz as KBC clock input.

               = 01 Select 8MHz as KBC clock input.

               = 10 Select 12Mhz as KBC clock input.

               = 11 Select 16Mhz as KBC clock input.

               (W83627HF/F-AW can support these 4 kinds of clock input, but W83627HF/F-PW only support 12MHz clock input)

    Bit 5 - 3  : Reserved.

    Bit 2      = 0 Port 92 disable.

               = 1 Port 92 enable.

    Bit 1      = 0 Gate20 software control.

               = 1 Gate20 hardware speed up.

    Bit 0      = 0 KBRST software control.

               = 1 KBRST hardware speed up.

## 4.7 Logical Device 6 (CIR)

**CR30 (Default 0x00)**

    Bit 7 - 1  : Reserved.

    Bit 0      = 1 Activates the logical device.

               = 0 Logical device is inactive.

**CR60, CR 61 (Default 0x00, 0x00)**

    These two registers select CIR I/O base address [0x100:0xFF8] on 8 byte boundary.

**CR70 (Default 0x00)**

    Bit 7 - 4  : Reserved.

    Bit [3:0]  : These bits select IRQ resource for CIR.

## 4.8 Logical Device 7 (Game Port and MIDI Port and GPIO Port 1)

**CR30 (Default 0x00)**

    Bit 7 - 3  : Reserved

    Bit 2      =1 Only MIDI Port Active. (Only For J version)

               =0 Only MIDI Port Disable.

    Bit 1      =1 Only Game Port Active. (Only For J version)

               =0 Only Game Port Disable.

    Bit 0      = 1 Activate Game Port, MIDI Port, and GPIO Function.

               = 0 Game Port and MIDI Port is inactive.

**CR60, CR 61 (Default 0x02, 0x01 if PNPCVS = 0 during POR, default 0x00 otherwise)**

    These two registers select the Game Port base address [0x100:0xFFF] on 1 byte boundary.

**CR62, CR 63 (Default 0x03, 0x30 if PNPCVS = 0 during POR, default 0x00 otherwise)**
These two registers select the MIDI Port base address [0x100:0xFFF] on 2 byte boundary.

**CR70 (Default 0x09 if PNPCVS = 0 during POR, default 0x00 otherwise)**
Bit 7 - 4 : Reserved.
Bit [3:0] : These bits select IRQ resource for MIDI Port .

**CRF0 (GP10-GP17 I/O selection register.  Default 0xFF)**
When set to a '1', respective GPIO port is programmed as an input port.
When set to a '0', respective GPIO port is programmed as an output port.

**CRF1 (GP10-GP17 data register.  Default 0x00)**
If  a port is programmed to be an output port, then its respective bit can be read/written.
If  a port is programmed to be an input port, then its respective bit can only be read.

**CRF2 (GP10-GP17 inversion register.  Default 0x00)**
When set to a '1', the incoming/outgoing port value is inverted.
When set to a '0', the incoming/outgoing port value is the same as in data register.

**CRF3 ( MIDI FIFO Threshold Setting. Default 0x00) (Only for J Version)**
= 00   1  byte
= 01   4  bytes
= 10   8  bytes
= 11  14 bytes

## 4.9 Logical Device 8 (GPIO Port 2)

**CR30 (GP20-GP27 Default 0x00)**
Bit 7 - 1 : Reserved.
Bit 0      = 1 Activate GPIO2.
               = 0 GPIO2 is inactive.

**CRF0 (GP20-GP27 I/O selection register.  Default 0xFF)**
When set to a '1', respective GPIO port is programmed as an input port.
When set to a '0', respective GPIO port is programmed as an output port.

**CRF1 (GP20-GP27 data register.  Default 0x00)**
If a port is programmed to be an output port, then its respective bit can be read/written.
If a port is programmed to be an input port, then its respective bit can only be read.

**CRF2 (GP20-GP27 inversion register.  Default 0x00)**
When set to a '1', the incoming/outgoing port value is inverted.
When set to a '0', the incoming/outgoing port value is the same as in data register.

**CRF3 (Default 0x00)**

    Bit 7 - 4  : These bits select IRQ resource for IRQIN1.

    Bit 3 - 0  : These bits select IRQ resource for IRQIN0.

**CRF4 (Reserved)**

**CRF5 (PLED mode register.  Default 0x00)**

    Bit 7-6    : select PLED mode

                = 00    Power LED pin is tri-stated.

                = 01    Power LED pin is drived low.

                = 10    Power LED pin is a 1Hz toggle pulse with 50 duty cycle

                = 11    Power LED pin is a 1/4Hz toggle pulse with 50 duty cycle.

    Bit 5-4    : Reserved

    Bit 3       : select WDTO count mode.

                = 0     second

                = 1     minute

    Bit 2       : Enable the rising edge of keyboard Reset(P20) to force Time-out event.

                = 0    Disable

                = 1    Enable

    Bit 1-0    : Reserved

**CRF6 (Default 0x00)**

Watch Dog Timer Time-out value.  Writing a non-zero value to this register causes the counter to load the value to Watch Dog Counter and start counting down.  If the Bit 7 and Bit 6 are set, any Mouse Interrupt or Keyboard Interrupt event will also cause the reload of previously-loaded non-zero value to Watch Dog Counter and start counting down.  Reading this register returns current value in Watch Dog Counter instead of Watch Dog Timer Time-out value.

    Bit 7 - 0  = 0x00 Time-out Disable

                = 0x01 Time-out occurs after 1 second/minute

                = 0x02 Time-out occurs after 2 second/minutes

                = 0x03 Time-out occurs after 3 second/minutes

                ……………………………………………

                = 0xFF Time-out occurs after 255 second/minutes

**CRF7 (Default 0x00)**

    Bit 7      : Mouse interrupt reset Enable or Disable
               = 1    Watch Dog Timer is reset upon a Mouse interrupt
               = 0    Watch Dog Timer is not affected by Mouse interrupt
    Bit 6      : Keyboard interrupt reset Enable or Disable
               = 1    Watch Dog Timer is reset upon a Keyboard interrupt
               = 0    Watch Dog Timer is not affected by Keyboard interrupt
    Bit 5      : Force Watch Dog Timer Time-out, Write only
               = 1    Force Watch Dog Timer time-out event; this bit is self-clearing.
    Bit 4      : Watch Dog Timer Status, R/W
               = 1    Watch Dog Timer time-out occurred
               = 0    Watch Dog Timer counting
    Bit 3 -0   : These bits select IRQ resource for Watch Dog.  Setting of 2 selects SMI.


## 4.10 Logical Device 9 (GPIO Port 3 This power of the Port is standby source (VSB) )

**CR30 (Default 0x00)**

    Bit 7 - 1  : Reserved
    Bit 0      = 1 Activate GPIO3.
               = 0 GPIO3 is inactive.


**CRF0 (GP30-GP35 I/O selection register.  Default 0xFF Bit 7-6: Reserve)**

When set to a '1', respective GPIO port is programmed as an input port.
When set to a '0', respective GPIO port is programmed as an output port.


**CRF1 (GP30-GP35 data register.  Default 0x00 Bit 7-6: Reserve)**

If  a port is programmed to be an output port, then its respective bit can be read/written.
If  a port is programmed to be an input port, then its respective bit can only be read.


**CRF2 (GP30-GP35 inversion register.  Default 0x00 Bit 7-6: Reserve)**

When set to a '1', the incoming/outgoing port value is inverted.
When set to a '0', the incoming/outgoing port value is the same as in data register.


**CRF3 (SUSLED mode register.  Default 0x00)**

    Bit 7-6    : select Suspend LED mode
               = 00    Suspend LED pin is drived low.
               = 01    Suspend LED pin is tri-stated.
               = 10    Suspend LED pin is a 1Hz toggle pulse with 50 duty cycle.
               = 11    Suspend LED pin is a 1/4Hz toggle pulse with 50 duty cycle.
    This mode selection bit 7-6 keep its settings until battery power loss.
    Bit 5 - 0  : Reserved.

## 4.11 Logical Device A (ACPI)

**CR30 (Default 0x00)**

Bit 7 - 1 : Reserved.

Bit 0 = 1 Activates the logical device.

= 0 Logical device is inactive.

**CR70 (Default 0x00)**

Bit 7 - 4 : Reserved.

Bit 3 - 0 : These bits select IRQ resources for $\overline{PME}$ .

**CRE0 (Default 0x00)**

Bit 7 : DIS-PANSW_IN. Disable panel switch input to turn system power supply on.

= 0 PANSW_IN is wire-ANDed and connected to PANSW_OUT.

= 1 PANSW_IN is blocked and can not affect PANSW_OUT.

Bit 6 : ENKBWAKEUP. Enable Keyboard to wake-up system via PANSW_OUT.

= 0 Disable Keyboard wake-up function.

= 1 Enable Keyboard wake-up function.

Bit 5 : ENMSWAKEUP. Enable Mouse to wake-up system via PANSW_OUT.

= 0 Disable Mouse wake-up function.

= 1 Enable Mouse wake-up function.

Bit 4 : MSRKEY. Select Mouse Left/Right Botton to wake-up system via PANSW_OUT.

= 0 Select click on Mouse Left-botton twice to wake the system up.

= 1 Select click on Mouse right-botton twice to wake the system up.

Bit 3 : ENCIRWAKEUP. Enable CIR to wake-up system via PANSW_OUT.

= 0 Disable CIR wake-up function.

= 1 Enable CIR wake-up function.

Bit 2 : KB/MS Swap. Enable Keyboard/Mouse port-swap.

= 0 Keyboard/Mouse ports are not swapped.

= 1 Keyboard/Mouse ports are swapped.

Bit 1 : MSXKEY. Enable any character received from Mouse to wake-up the system.

= 0 Only click Mouse left/right-botton twice can wake the system up.

= 1 Only click Mouse left/right-botton once can wake the system up.

Bit 0 : KBXKEY. Enable any character received from Keyboard to wake-up the system

= 0 Only predetermined specific key combination can wake up the system.

= 1 Any character received from Keyboard can wake up the system.

**CRE1 (Default 0x00) Keyboard Wake-Up Index Register**

This register is used to indicate which Keyboard Wake-Up Shift register or Predetermined key Register is to be read/written via CRE2. The range of Keyboard wake-up index register is 0x00 - 0x19, and the range of CIR wake-up index register is 0x20 - 0x2F.

**CRE2 Keyboard Wake-Up Data Register**

This register holds the value of wake-up key register indicated by CRE1. This register can be read/written.

**CRE3 (Read only) Keyboard/Mouse Wake-Up Status Register**

Bit 7-6 : Reserved.

Bit 5 : When 1 is VSB Power Loss status.

Bit 4 :PWRLOSS_STS: This bit is set when power loss occurs. This bit is control by CR E4, bit 7

Bit 3 :CIR_STS. The Panel switch event is caused by CIR wake-up event. This bit is cleared by reading this register.

Bit 2 :PANSW_STS. The Panel switch event is caused by PANSW_IN. This bit is cleared by reading this register.

Bit 1 :Mouse_STS. The Panel switch event is caused by Mouse wake-up event. This bit is cleared by reading this register.

Bit 0 :Keyboard_STS. The Panel switch event is caused by Keyboard wake-up event. This bit is cleared by reading this register.

**CRE4 (Default 0x00)**

Bit 7 : Power loss control bit 2.

0 = Disable ACPI resume

1 = Enable ACPI resume

Bit 6-5 : Power loss control bit <1:0>

00 = System always turn off when come back from power loss state.

01 = System always turn on when come back from power loss state.

10 = System turn on/off when come back from power loss state depend on the state before power loss.

11 = Reserved.

Bit 4 : Suspend clock source select

0 = Use internal clock source.

1 = Use external suspend clock source(32.768KHz).

Bit 3 : Keyboard wake-up type select for wake-up the system from S1/S2.

0 = Password or Hot keys programmed in the registers.

1 =Any key.

Bit 2 : Enable all wake-up event set in CRE0 can wake-up the system from S1/S2 state. This bit is cleared when wake-up event occurs.

0 = Disable.

1 = Enable.

Bit 1 - 0 : Reserved.

**CRE5 (Default 0x00)**

Bit 7 : Reserved

Bit 6 - 0 : Compared Code Length. When the compared codes are stored in the data register, these data length should be written to this register.

**CRE6 (Default 0x00)**

Bit 7 : EMDATUP  enable Mouse any key wake up.

Bit 6 : Reserved

Bit 5 - 0 : CIR Baud Rate Divisor. The clock base of CIR is 32khz, so that the baud rate is 32khz divided by ( CIR Baud Rate Divisor + 1).

**CRE7 (Default 0x00)**

Bit 7 : ENKD3. Enable third wake up key set.

Bit 6 : ENKD2. Enable second wake up key set.

Bit 5 : Enable Win98 direct key to wake up the system.

Bit 4 : EN_ONPSOUT. Set this bit will make PSOUT# issue a 0.5 Second pulse when system returns from power loss.

Bit 3 : SELWDTORST. Watch Dog Timer Reset Control.

= 0 is reset by LPC_RST.

= 1 is reset by PWR_OK.

Bit 2 : Reset CIR Power-On function. After using CIR power-on, the software should write logical 1 to restart CIR power-on function.

Bit 1 : Invert RX Data.

= 1 Inverting RX Data.

= 0 Not inverting RX Data.

Bit 0 : Enable Demodulation.

= 1 Enable received signal to demodulate.

= 0 Disable received signal to demodulate.

**CRF0 (Default 0x00)**

Bit 7 : CHIPPME.  Chip level auto power management enable.

= 0disable the auto power management functions

= 1enable the auto power management functions.

Bit 6 : CIRPME.  Consumer IR port auto power management enable.

= 0disable the auto power management functions

= 1enable the auto power management functions.

Bit 5 : MIDIPME.  MIDI port auto power management enable.

= 0disable the auto power management functions

= 1enable the auto power management functions.

Bit 4 : Reserved.  Return zero when read.

Bit 3 : PRTPME.  Printer port auto power management enable.

= 0disable the auto power management functions.

= 1enable the auto power management functions.

Bit 2     : FDCPME.  FDC auto power management enable.

      = 0disable the auto power management functions.

      = 1enable the auto power management functions.

Bit 1     : URAPME.  UART A auto power management enable.

      = 0disable the auto power management functions.

      = 1enable the auto power management functions.

Bit 0     : URBPME.  UART B auto power management enable.

      = 0disable the auto power management functions.

      = 1enable the auto power management functions.

## CRF1 (Default 0x00)

Bit 7     : WAK_STS. This bit is set when the chip is in the sleeping state and an enabled resume event occurs. Upon setting this bit, the sleeping/working state machine will transition the system to the working state. This bit is only set by hardware and is cleared by writing a 1 to this bit position or by the sleeping/working state machine automatically when the global standby timer expires.

      = 0     the chip is in the sleeping state.

      = 1     the chip is in the working state.

Bit 6 - 5  : Devices' trap status.

Bit 4     : Reserved.  Return zero when read.

Bit 3 - 0  : Devices' trap status.

## CRF3 (Default 0x00)

Bit 7 - 6  : Reserved.  Return zero when read.

Bit 5 - 0  : Device's IRQ status.

      These bits indicate the IRQ status of the individual device respectively.  The device's IRQ status bit is set by their source device and is cleared by writing a 1.  Writing a 0 has no effect.

Bit 5     : MOUIRQSTS.  MOUSE IRQ status.

Bit 4     : KBCIRQSTS.  KBC IRQ status.

Bit 3     : PRTIRQSTS. printer port IRQ status.

Bit 2     : FDCIRQSTS. FDC IRQ status.

Bit 1     : URAIRQSTS. UART A IRQ status.

Bit 0     : URBIRQSTS. UART B IRQ status.

**CRF4 (Default 0x00)**

    Bit 7 - 6  : Reserved.  Return zero when read.

    Bit 5 - 0  : These bits indicate the IRQ status of the individual GPIO function or logical device respectively. The status bit is set by their source function or device and is cleared by writing a1. Writing a 0 has no effect.

    Bit 5     : HMIRQSTS. Hardware monitor IRQ status.

    Bit 4     : WDTIRQSTS. Watch dog timer IRQ status.

    Bit 3     : CIRIRQSTS. Consumer IR IRQ  status.

    Bit 1     : IRQIN1STS. IRQIN1 status.

    Bit 0     : IRQIN0STS. IRQIN0 status.

**CRF6 (Default 0x00)**

    Bit 7 - 6  : Reserved.  Return zero when read.

    Bit 5 - 0  : Enable bits of the $\overline{SMI}/\overline{PME}$ generation due to the device's IRQ.

These bits enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to any IRQ of the devices.

$\overline{SMI}/\overline{PME}$ logic output = (MOUIRQEN and MOUIRQSTS) or (KBCIRQEN and KBCIRQSTS)  or (PRTIRQEN and PRTIRQSTS) or (FDCIRQEN and FDCIRQSTS)   or (URAIRQEN and URAIRQSTS) or (URBIRQEN and URBIRQSTS) or (HMIRQEN and HMIRQSTS) or (WDTIRQEN and WDTIRQSTS) or (IRQIN3EN and IRQIN3STS) or (IRQIN2EN and IRQIN2STS) or (IRQIN1EN and IRQIN1STS) or (IRQIN0EN and IRQIN0STS)

    Bit 5     : MOUIRQEN.

        = 0disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to MOUSE's IRQ.

        = 1enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to MOUSE's IRQ.

    Bit 4     : KBCIRQEN.

        = 0disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to KBC's IRQ.

        = 1enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to KBC's IRQ.

    Bit 3     : PRTIRQEN.

        = 0disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to printer port's IRQ.

        = 1enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to printer port's IRQ.

    Bit 2     : FDCIRQEN.

        = 0disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to FDC's IRQ.

        = 1enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to FDC's IRQ.

    Bit 1     : URAIRQEN.

        = 0disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to UART A's IRQ.

        = 1enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to UART A's IRQ.

    Bit 0     : URBIRQEN.

        = 0disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to UART B's IRQ.

        = 1enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to UART B's IRQ.

**CRF7 (Default 0x00)**

    Bit 7 - 6  : Reserved.  Return zero when read

    Bit 5 - 0  : Enable bits of the $\overline{SMI}$ / $\overline{PME}$ generation due to the GPIO IRQ function or device's IRQ.

    Bit 5     : HMIRQEN.

           = 0disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to hardware monitor's IRQ.

           = 1enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to hardware monitor's IRQ.

    Bit 4     : WDTIRQEN.

           = 0disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to watch dog timer's IRQ.

           = 1enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to watch dog timer's IRQ.

    Bit 3     : CIRIRQEN.

           = 0disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to CIR's IRQ.

           = 1enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to CIR's IRQ

    Bit 2     : MIDIIRQEN.

           = 0disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to MIDI's IRQ.

           = 1enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to MIDI's IRQ.

    Bit 1     : IRQIN1EN.

           = 0disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to IRQIN1's IRQ.

           = 1enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to IRQIN1's IRQ.

    Bit 0     : IRQIN0EN.

           = 0disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to IRQIN0's IRQ.

           = 1enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to IRQIN0's IRQ.

**CRF9 (Default 0x00)**

    Bit 7 - 3  : Reserved. Return zero when read.

    Bit 2     : PME_EN: Select the power management events to be either an $\overline{PME}$ or $\overline{SMI}$ interrupt for the IRQ events. Note that: this bit is valid only when SMIPME_OE = 1.

           = 0     the power management events will generate an $\overline{SMI}$ event

           = 1     the power management events will generate an $\overline{PME}$ event.

    Bit 1     : FSLEEP: This bit selects the fast expiry time of individual devices.

           = 0     1 second.

           = 1     8 milli-seconds

    Bit 0     : SMIPME_OE: This is the $\overline{SMI}$ and $\overline{PME}$ output enable bit.

           = 0     neither $\overline{SMI}$ nor $\overline{PME}$ will be generated. Only the IRQ status bit is set.

           = 1     an $\overline{SMI}$ or $\overline{PME}$ event will be generated.

**CRFE, FF (Default 0x00)**

       Reserved for Winbond test.

## W83627HF/F

### 4.12 Logical Device B (Hardware Monitor)

**CR30 (Default 0x00)**

Bit 7 - 1 : Reserved.

Bit 0 = 1 Activates the logical device.

= 0 Logical device is inactive.

**CR60, CR 61 (Default 0x00, 0x00)**

These two registers select Hardware Monitor base address [0x100:0xFFF] on 8-byte boundary.

**CR70 (Default 0x00)**

Bit 7 - 4 : Reserved.

Bit 3 - 0 : These bits select IRQ resource for Hardware Monitor.

**CRF0 (Default 0x00)**

Bit 7 - 1 : Reserved.

Bit 0 : Disable initial abnormal beep (VcoreA and +3.3 V)

= 0 Enable power-on abnormal beep

= 1 Disable power-on abnormal beep

## 5. SPECIFICATIONS

### 5.1 Absolute Maximum Ratings

| PARAMETER | RATING | UNIT |
|---|---|---|
| Power Supply Voltage (5V) | -0.5 to 7.0 | V |
| Input Voltage | -0.5 to $V_{DD}$+0.5 | V |
| RTC Battery Voltage $V_{BAT}$ | 2.2 to 4.0 | V |
| Operating Temperature | 0 to +70 | ° C |
| Storage Temperature | -55 to +150 | ° C |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

### 5.2 DC CHARACTERISTICS

(Ta = 0° C to 70° C, $V_{DD}$ = 5V $\pm$ 10%, $V_{SS}$ = 0V)

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| RTC Battery Quiescent Current | $I_{BAT}$ | | | 2.4 | uA | $V_{BAT}$ = 2.5 V |
| ACPI Stand-by Power Supply Quiescent Current | $I_{BAT}$ | | | 2.0 | mA | $V_{SB}$ = 5.0 V, All ACPI pins are not connected. |
| **I/O$_{8t}$ - TTL level bi-directional pin with 8mA source-sink capability** | | | | | | |
| Input Low Voltage | $V_{IL}$ | | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | | | V | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 8 mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = - 8 mA |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = 5V |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0V |
| **I/O$_{12t}$ - TTL level bi-directional pin with 12mA source-sink capability** | | | | | | |
| Input Low Voltage | $V_{IL}$ | | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | | | V | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 12 mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -12 mA |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = 5V |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0V |

5.2  DC CHARACTERISTICS, continued

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| **I/O$_{24t}$ - TTL level bi-directional pin with 24mA source-sink capability** | | | | | | |
| Input Low Voltage | V$_{IL}$ | | | 0.8 | V | |
| Input High Voltage | V$_{IH}$ | 2.0 | | | V | |
| Output Low Voltage | V$_{OL}$ | | | 0.4 | V | I$_{OL}$ = 24 mA |
| Output High Voltage | V$_{OH}$ | 2.4 | | | V | I$_{OH}$ = -24 mA |
| Input High Leakage | I$_{LIH}$ | | | +10 | μA | V$_{IN}$ = 5V |
| Input Low Leakage | I$_{LIL}$ | | | -10 | μA | V$_{IN}$ = 0V |
| **I/O$_{12tp3}$ – 3.3V TTL level bi-directional pin with 12mA source-sink capability** | | | | | | |
| Input Low Voltage | V$_{IL}$ | | | 0.8 | V | |
| Input High Voltage | V$_{IH}$ | 2.0 | | | V | |
| Output Low Voltage | V$_{OL}$ | | | 0.4 | V | I$_{OL}$ = 12 mA |
| Output High Voltage | V$_{OH}$ | 2.4 | | | V | I$_{OH}$ = -12 mA |
| Input High Leakage | I$_{LIH}$ | | | +10 | μA | V$_{IN}$ = 3.3V |
| Input Low Leakage | I$_{LIL}$ | | | -10 | μA | V$_{IN}$ = 0V |
| **I/O$_{12ts}$ - TTL level Schmitt-trigger bi-directional pin with 12mA source-sink capability** | | | | | | |
| Input Low Threshold Voltage | V$_{t-}$ | 0.5 | 0.8 | 1.1 | V | |
| Input High Threshold Voltage | V$_{t+}$ | 1.6 | 2.0 | 2.4 | V | |
| Hystersis | V$_{TH}$ | 0.5 | 1.2 | | V | V$_{DD}$=5V |
| Output Low Voltage | V$_{OL}$ | | | 0.4 | V | I$_{OL}$ = 12 mA |
| Output High Voltage | V$_{OH}$ | 2.4 | | | V | I$_{OH}$ = -12 mA |
| Input High Leakage | I$_{LIH}$ | | | +10 | μA | V$_{IN}$ = 5V |
| Input Low Leakage | I$_{LIL}$ | | | -10 | μA | V$_{IN}$ = 0V |
| **I/O$_{24ts}$ - TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability** | | | | | | |
| Input Low Threshold Voltage | V$_{t-}$ | 0.5 | 0.8 | 1.1 | V | |
| Input High Threshold Voltage | V$_{t+}$ | 1.6 | 2.0 | 2.4 | V | |
| Hystersis | V$_{TH}$ | 0.5 | 1.2 | | V | V$_{DD}$=5V |
| Output Low Voltage | V$_{OL}$ | | | 0.4 | V | I$_{OL}$ = 24 mA |
| Output High Voltage | V$_{OH}$ | 2.4 | | | V | I$_{OH}$ = -24 mA |
| Input High Leakage | I$_{LIH}$ | | | +10 | μA | V$_{IN}$ = 5V |

5.2 DC CHARACTERISTICS, continued

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0V |
| **I/O$_{24tsp3}$ – 3.3V TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability** | | | | | | |
| Input Low Threshold Voltage | $V_{t-}$ | 0.5 | 0.8 | 1.1 | V | |
| Input High Threshold Voltage | $V_{t+}$ | 1.6 | 2.0 | 2.4 | V | |
| Hystersis | $V_{TH}$ | 0.5 | 1.2 | | V | $V_{DD}$=3.3V |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 24 mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -24 mA |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = 3.3V |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0V |
| **I/OD$_{12t}$ - TTL level bi-directional pin and open-drain output with 12mA sink capability** | | | | | | |
| Input Low Voltage | $V_{IL}$ | | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | | | V | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 12 mA |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = 5V |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0V |
| **I/OD$_{24t}$ - TTL level bi-directional pin and open-drain output with 24mA sink capability** | | | | | | |
| Input Low Voltage | $V_{IL}$ | | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | | | V | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 24 mA |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = 5V |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0V |
| **I/OD$_{12ts}$ - TTL level Schmitt-trigger bi-directional pin and open drain output with 12mA sink capability** | | | | | | |
| Input Low Threshold Voltage | $V_{t-}$ | 0.5 | 0.8 | 1.1 | V | |
| Input High Threshold Voltage | $V_{t+}$ | 1.6 | 2.0 | 2.4 | V | |
| Hystersis | $V_{TH}$ | 0.5 | 1.2 | | V | $V_{DD}$=5V |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 12 mA |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = 5V |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0V |

5.2  DC CHARACTERISTICS, continued

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| Hystersis | $V_{TH}$ | 1.5 | 2 | | V | $V_{DD}$ = 5 V |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 12 mA |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = 5V |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0 V |
| **I/OD12$_{csu}$ - CMOS level Schmitt-trigger bi-directional pin with internal pull up resistor and open drain output with 12mA sink capability** | | | | | | |
| Input Low Threshold Voltage | $V_{t-}$ | 1.3 | 1.5 | 1.7 | V | $V_{DD}$ = 5 V |
| Input High Threshold Voltage | $V_{t+}$ | 3.2 | 3.5 | 3.8 | V | $V_{DD}$ = 5 V |
| Hystersis | $V_{TH}$ | 1.5 | 2 | | V | $V_{DD}$ = 5 V |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 12 mA |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = 5V |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0 V |
| **O4 - Output pin with 4mA source-sink capability** | | | | | | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 4 mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -4 mA |
| **O8 - Output pin with 8mA source-sink capability** | | | | | | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 8 mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -8 mA |
| **O12 - Output pin with 12mA source-sink capability** | | | | | | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 12 mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -12 mA |
| **O16 - Output pin with 16mA source-sink capability** | | | | | | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 16 mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -16 mA |

5.2 DC CHARACTERISTICS, continued

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| **O24 - Output pin with 24mA source-sink capability** | | | | | | |
| Output Low Voltage | VOL | | | 0.4 | V | IOL = 24 mA |
| Output High Voltage | VOH | 2.4 | | | V | IOH = -24 mA |
| **O12p3 - 3.3V output pin with 12mA source-sink capability** | | | | | | |
| Output Low Voltage | VOL | | | 0.4 | V | IOL = 12 mA |
| **O24p3 - 3.3V output pin with 24mA source-sink capability** | | | | | | |
| Output Low Voltage | VOL | | | 0.4 | V | IOL = 24 mA |
| **OD12 - Open drain output pin with 12mA sink capability** | | | | | | |
| Output Low Voltage | VOL | | | 0.4 | V | IOL = 12 mA |
| **OD24 - Open drain output pin with 24mA sink capability** | | | | | | |
| Output Low Voltage | VOL | | | 0.4 | V | IOL = 24 mA |
| **OD12p3 - 3.3V open drain output pin with 12mA sink capability** | | | | | | |
| Output Low Voltage | VOL | | | 0.4 | V | IOL = 12 mA |
| **INt - TTL level input pin** | | | | | | |
| Input Low Voltage | VIL | | | 0.8 | V | |
| Input High Voltage | VIH | 2.0 | | | V | |
| Input High Leakage | ILIH | | | +10 | μA | VIN = 5V |
| Input Low Leakage | ILIL | | | -10 | μA | VIN = 0 V |
| **INtp3 - 3.3V TTL level input pin** | | | | | | |
| Input Low Voltage | VIL | | | 0.8 | V | |
| Input High Voltage | VIH | 2.0 | | | V | |
| Input High Leakage | ILIH | | | +10 | μA | VIN = 3.3V |
| Input Low Leakage | ILIL | | | -10 | μA | VIN = 0 V |
| **INtd - TTL level input pin with internal pull down resistor** | | | | | | |
| Input Low Voltage | VIL | | | 0.8 | V | |
| Input High Voltage | VIH | 2.0 | | | V | |
| Input High Leakage | ILIH | | | +10 | μA | VIN = 5V |
| Input Low Leakage | ILIL | | | -10 | μA | VIN = 0 V |
| **INtu - TTL level input pin with internal pull up resistor** | | | | | | |
| Input Low Voltage | VIL | | | 0.8 | V | |

5.2 DC CHARACTERISTICS, continued

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | 2.0 | | | V | |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN} = 5V$ |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN} = 0$ V |
| **$IN_{ts}$ - TTL level Schmitt-trigger input pin** | | | | | | |
| Input Low Threshold Voltage | $V_{t-}$ | 0.5 | 0.8 | 1.1 | V | $V_{DD} = 5$ V |
| Input High Threshold Voltage | $V_{t+}$ | 1.6 | 2.0 | 2.4 | V | $V_{DD} = 5$ V |
| Hystersis | $V_{TH}$ | 0.5 | 1.2 | | V | $V_{DD} = 5$ V |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN} = 5V$ |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN} = 0$ V |
| **$IN_{tsp3}$ - 3.3 V TTL level Schmitt-trigger input pin** | | | | | | |
| Input Low Threshold Voltage | $V_{t-}$ | 0.5 | 0.8 | 1.1 | V | $V_{DD} = 3.3$ V |
| Input High Threshold Voltage | $V_{t+}$ | 1.6 | 2.0 | 2.4 | V | $V_{DD} = 3.3$ V |
| Hystersis | $V_{TH}$ | 0.5 | 1.2 | | V | $V_{DD} = 3.3$ V |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN} = 3.3$ V |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN} = 0$ V |
| **$IN_c$ - CMOS level input pin** | | | | | | |
| Input Low Voltage | $V_{IL}$ | | | 1.5 | V | |
| Input High Voltage | $V_{IH}$ | 3.5 | | | V | |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN} = 5V$ |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN} = 0$ V |
| **$IN_{cd}$ - CMOS level input pin with internal pull down resistor** | | | | | | |
| Input Low Voltage | $V_{IL}$ | | | 1.5 | V | |
| Input High Voltage | $V_{IH}$ | 3.5 | | | V | |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN} = 5V$ |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN} = 0$ V |
| **$IN_{cs}$ - CMOS level Schmitt-trigger input pin** | | | | | | |
| Input Low Threshold Voltage | $V_{t-}$ | 1.3 | 1.5 | 1.7 | V | $V_{DD} = 5$ V |

5.2  DC CHARACTERISTICS, continued

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| Hystersis | $V_{TH}$ | 1.5 | 2 | | V | $V_{DD} = 5$ V |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN} = 5$ V |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN} = 0$ V |
| **$IN_{csu}$ - CMOS level Schmitt-trigger input pin with internal pull up resistor** | | | | | | |
| Input Low Threshold Voltage | $V_{t-}$ | 1.3 | 1.5 | 1.7 | V | $V_{DD} = 5$ V |
| Input High Threshold Voltage | $V_{t+}$ | 3.2 | 3.5 | 3.8 | V | $V_{DD} = 5$ V |
| Hystersis | $V_{TH}$ | 1.5 | 2 | | V | $V_{DD} = 5$ V |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN} = 5V$ |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN} = 0$ V |

# 6. APPLICATION CIRCUITS

## 6.1 Parallel Port Extension FDD



**Parallel Port Extension FDD Mode Connection Diagram**

## 6.2 Parallel Port Extension 2FDD

JP13

WE2/SLCT — 13
WD2/PE — 25 / 12
MOB2/BUSY — 24 / 11
DSB2/ACK — 23 / 10
DSA2/PD7 — 22 / 9
MOA2/PD6 — 21 / 8
PD5 — 20 / 7
DCH2/PD4 — 19 / 6
RDD2/PD3 — 18 / 5
STEP2/SLIN — 17
WP2/PD2 — 4
DIR2/INIT — 16
TRK02/PD1 — 3
HEAD2/ERR — 15 / 2
IDX2/PD0 — 14
RWC2/AFD — 1
STB

PRINTER PORT

JP 13A

DCH2 — 34 / 33
HEAD2 — 32 / 31
RDD2 — 30 / 29
WP2 — 28 / 27
TRK02 — 26 / 25
WE2 — 24 / 23
WD2 — 22 / 21
STEP2 — 20 / 19
DIR2 — 18 / 17
MOB2 — 16 / 15
DSA2 — 14 / 13
DSB2 — 12 / 11
MOA2 — 10 / 9
IDX2 — 8 / 7
6 / 5
4 / 3
RWC2 — 2 / 1

EXT FDC

**Parallel Port Extension 2FDD Connection Diagram**

## 6.3 Four FDD Mode

W83977F

DSA
DSB
MOA
MOB

74LS139

G1
A1
B1

G2
A2
B2

1Y0
1Y1
1Y2
1Y3
2Y0
2Y1
2Y2
2Y3

7407(2)

DSA
DSB
DSC
DSD
MOA
MOB
MOC
MOD

## 7. ORDERING INSTRUCTION

| PART NO. | KBC FIRMWARE | REMARKS |
|---|---|---|
| W83627HF-AW | AMIKEY-2<sup>TM</sup> | |
| W83627HF-PW | Phoenix MultiKey/42<sup>TM</sup> | Only support 12MHz KBC clock input |

## 8. HOW TO READ THE TOP MARKING

Example: The top marking of W83627HF-AW



1st line: Winbond logo
2nd line: the type number: W83627HF-AW

3rd line: the source of KBC F/W -- American Megatrends Incorporated<sup>TM</sup>
4th line: the tracking code    821  A 2 C 282012345BC

     **821**:  packages made in '9<u>8</u>, week <u>21</u>
     **A**:  assembly house ID; A means ASE, S means SPIL.... etc.
     **2**:   Winbond internal use.
     **B**:  IC revision; A means version A, B means version B
     **282012345**:  wafer production series lot number
     **BC**:  Winbond internal use.

## 9. PACKAGE DIMENSIONS

**(128-pin QFP)**



| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A₁ | 0.25 | 0.35 | 0.45 | 0.010 | 0.014 | 0.018 |
| A₂ | 2.57 | 2.72 | 2.87 | 0.101 | 0.107 | 0.113 |
| b | 0.10 | 0.20 | 0.30 | 0.004 | 0.008 | 0.012 |
| c | 0.10 | 0.15 | 0.20 | 0.004 | 0.006 | 0.008 |
| D | 13.90 | 14.00 | 14.10 | 0.547 | 0.551 | 0.555 |
| E | 19.90 | 20.00 | 20.10 | 0.783 | 0.787 | 0.791 |
| e | — | 0.50 | — | — | 0.020 | — |
| H_D | 17.00 | 17.20 | 17.40 | 0.669 | 0.677 | 0.685 |
| H_E | 23.00 | 23.20 | 23.40 | 0.905 | 0.913 | 0.921 |
| L | 0.65 | 0.80 | 0.95 | 0.025 | 0.031 | 0.037 |
| L₁ | — | 1.60 | — | — | 0.063 | — |
| y | — | — | 0.08 | — | — | 0.003 |
| θ | 0 | — | 7 | 0 | — | 7 |

**Note:**
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion .
3. Controlling dimension : Millimeter
4. General appearance spec. should be based on final visual inspection spec.
5. PCB layout please use the "mm".

# APPENDIX A : DEMO CIRCUIT

SUSPEND LED CIRCUIT

POWER LED CIRCUIT

BATTERY CIRCUIT

PANEL SWITCH

PS2 MOUSE

KEYBOARD

KEYLOCK

IOVSB CIRCUIT

OnNow or Wake_up function power

R26 OFF, D2,D3 ON: Wake_up fuction

R26 ON, D2,D3 OFF:NO Wake_up fuction

JP5:1-2 Clear CMOS

2-3 Enable ONNOW functions

WINBOND ELECTRONICS CORP.

Title
W83627HF CIRCUIT (LPC I/O + H/M)
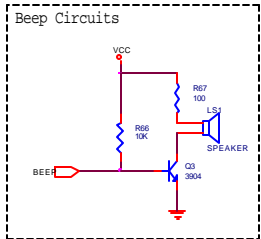
Size   Document Number
Custom KB & PS2 MOUSE & POWER                                      Rev 0.4

Date:    Monday, August 05, 2002          Sheet    2    of    6

# Winbond
## Electronics Corp.

# *W83627HF/F*



COM PORT

IR/CIR CONNECTOR

COMA (UARTA)

COMB (UARTB)

THE IOVSB OF PIN 8 IS FOR CIR WAKE-UP FUNCTION.

PRT PORT

| WINBOND ELECTRONICS CORP. | | | |
|---|---|---|---|
| Title | | | |
| W83627HF CIRCUIT (LPC I/O + H/W) | | | |
| Size | Document Number | | Rev |
| Custom | COM & IR & LPT PORT | | 0.4 |
| Date: | Monday, August 05, 2002 | Sheet   3   of   6 | |

GAME & MIDI PORT CIRCUIT
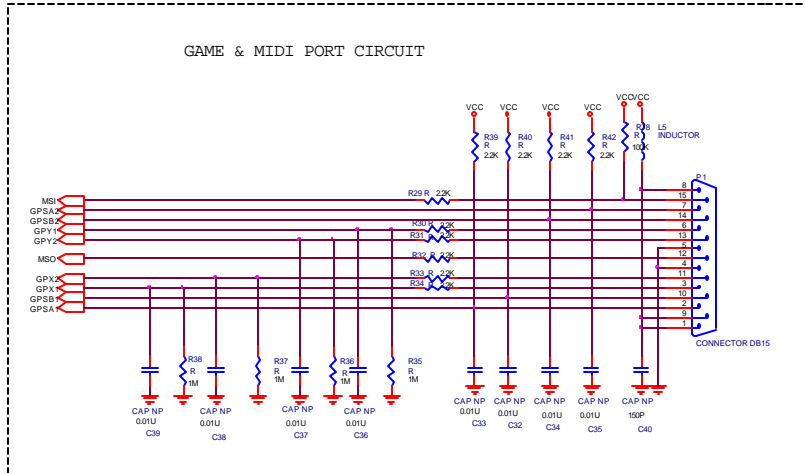
# W83627HF/F

## Hardware Monitor circuits

### Temperature Sensing



### Voltage Sensing



### PWM Circuit for FAN speed control



### Beep Circuits



### Case Open Circuits



### CPU Voltage ID output



### Fan Speed Input Circuit
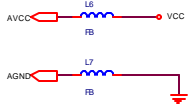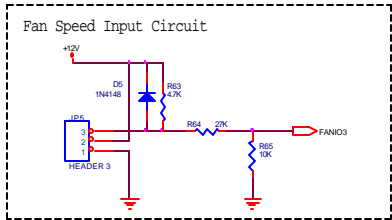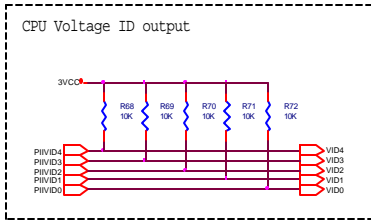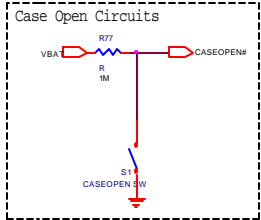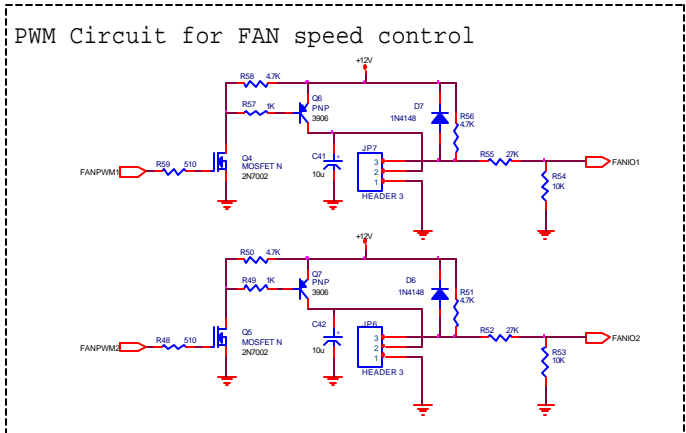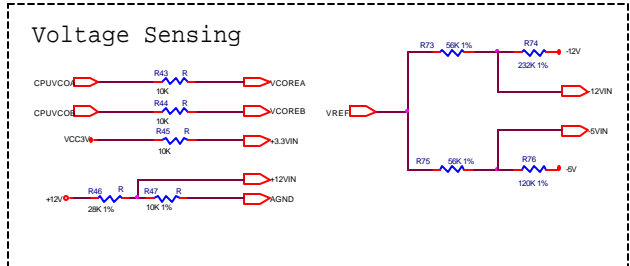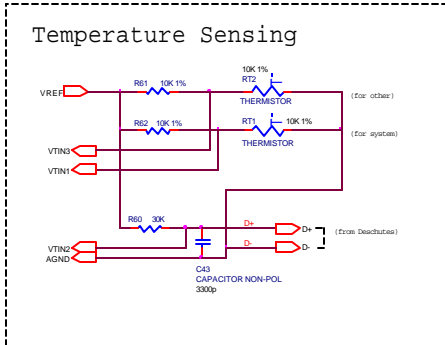


| Winbond Electronic Corp. | | | |
|---|---|---|---|
| Title | W83627HF CIRCUIT (LPC I/O+ H/W) | | |
| Size | Document Number | | Rev |
| Custom | Hardware Monitor | | 0.4 |
| Date: Monday, August 05, 2002 | Sheet 5 of 6 | | |